1. Record Nr. UNINA990007690770403321

Titolo	Digesto delle discipline penalistiche : diritto penale, diritto processuale penale, diritto penale del lavoro, diritto penale commerciale, diritto penale della navigazione, diritto penale tributario, diritto penale e processuale penale militari, diritto penale e processuale penale comparati, medicina legale e criminologia
Pubbl/distr/stampa	Torino : Utet, 1987
Descrizione fisica	v. ; 27 cm
Disciplina	340.03
Locazione	DDCP
Collocazione	22-C-III-1
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
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2. Record Nr. UNISA990000508320203316

Autore	CLEMENTE, Guido
Titolo	Guida alla storia romana / Guido Clemente
Pubbl/distr/stampa	Milano : A. Mondadori, 1988
ISBN	88-04-13873-4
Edizione	[5. ed.]
Descrizione fisica	446 p. ; 20 cm
Collana	Studo ; 49
Disciplina	937
Soggetti	Roma antica - Storia
Collocazione	IX.4. 24(Varie Coll 78/49) IX.4. 24a(Varie Coll 78/49 BIS)
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Livello bibliografico	Monografia
Note generali	In cop.: Eventi, strutture social, metodi di ricerca

3.	Record Nr.	UNINA9910484142403321
	Titolo	Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation : 22nd International Workshop, PATMOS 2012, Newcastle upon Tyne, UK, September 4-6, 2012, Revised Selected Papers / / edited by José L. Ayala, Delong Shang, Alex Yakovlev
	Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2013
	ISBN	3-642-36157-9
	Edizione	[1st ed. 2013.]
	Descrizione fisica	1 online resource (IX, 258 p. 150 illus.)
	Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 7606
	Altri autori (Persone)	AyalaJose L ShangDelong YakovlevAlex
	Disciplina	004.24
	Soggetti	Electronic digital computers - Evaluation Computer simulation Computer networks Computer hardware description languages Logic design Compilers (Computer programs) System Performance and Evaluation Computer Modelling Computer Communication Networks Register-Transfer-Level Implementation Logic Design Compilers and Interpreters
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Bibliographic Level Mode of Issuance: Monograph
	Nota di bibliografia	Includes bibliographical references and index.
	Nota di contenuto	Sleep-Transistor Based Power-Gating Tradeoff Analyses -- Modelling and Analysis of Manufacturing Variability Effects from Process to Architectural Level -- Non-invasive Power Simulation at System-Level with SystemC -- A Standard Cell Optimization Method for Near-Threshold Voltage Operations -- An Extended Metastability Simulation

Method for Synchronizer Characterization -- Phase Space Based NBTI Model -- Fast Propagation of Hamming and Signal Distances for Register-Transfer Level Datapaths -- Noise Margin Based Library Optimization Considering Variability in Sub-threshold -- TCP Window Based DVFS for Low Power Network Controller SoC -- A Generic Architecture for Robust Asynchronous Communication Links -- Direct Statistical Simulation of Timing Properties in Sequential Circuits -- On-Chip NBTI and PBTI Tracking through an All-Digital Aging Monitor Architecture -- Two-Phase MOBILE Interconnection Schemes for Ultra-Grain Pipeline Applications -- Design of a 150 mV Supply, 2 MIPS, 90nm CMOS, Ultra-Low-Power Microprocessor -- Run-Time Measurement of Harvested Energy for Autarkic Sensor Operation -- Observability Conditions and Automatic Operand-Isolation in High-Throughput Asynchronous Pipelines -- Dynamic Power Management of a Computer with Self Power-Managed Components -- Case Studies of Logical Computation on Stochastic Bit Streams.

Sommario/riassunto

This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design, PATMOS 2012, held in Newcastle, UK Spain, in September 2012. The 25 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems, including reconfigurable hardware such as FPGAs. The technical program focus on timing, performance and power consumption as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization.