1. Record Nr. UNISA990000336570203316

Titolo	Physics of the earth and planetary interiors : a journal devoted to observational and experimental studies of the chemistry and planetary interiors and their theoretical interpretation
Pubbl/distr/stampa	Amsterdam : Elsevier
ISSN	0031-9201
Descrizione fisica	v. : ill. ; 25 cm
Disciplina	551.05
Soggetti	Geologia -- Periodici
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Periodico
Note generali	Comincia nel 1967 Descrizione basata su: Vol.183, n.1(2010)

2. Record Nr. UNISA996465650903316

Titolo	Computer-Aided Verification [[electronic resource]] : 2nd Internatonal Conference, CAV '90, New Brunswick, NJ, USA, June 18-21, 1990. Proceedings / / edited by Edmund M. Clarke, Robert P. Kurshan
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 1991
ISBN	3-540-38394-8
Edizione	[1st ed. 1991.]
Descrizione fisica	1 online resource (XIV, 378 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 531
Disciplina	511.3
Soggetti	Mathematical logic Computers Computer logic Software engineering Special purpose computers Mathematical Logic and Foundations Theory of Computation Logics and Meanings of Programs Mathematical Logic and Formal Languages Software Engineering Special Purpose and Application-Based Systems
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Temporal logic model checking: Two techniques for avoiding the state explosion problem -- Automatic verification of extensions of hardware descriptions -- Papetri : Environment for the analysis of PETRI nets -- Verifying temporal properties of sequential machines without building their state diagrams -- Formal verification of digital circuits using symbolic ternary system models -- Vectorized model checking for computation tree logic -- to a computational theory and implementation of sequential hardware equivalence -- Auto/autograph -- A data path verifier for register transfer level using temporal logic language Tokio -- The use of model checking in ATPG for sequential circuits -- Compositional design and verification of communication

protocols, using labelled petri nets -- Issues arising in the analysis of L.0 -- Automated RTL verification based on predicate calculus -- On using protean to verify ISO FTAM protocol -- Quantitative temporal reasoning -- Using partial-order semantics to avoid the state explosion problem in asynchronous systems -- A stubborn attack on state explosion -- Using optimal simulations to reduce reachability graphs -- Using partial orders to improve automatic verification methods -- Compositional minimization of finite state systems -- Minimal model generation -- A context dependent equivalence relation between kripke structures -- The modular framework of computer-aided verification -- Verifying liveness properties by verifying safety properties -- Memory efficient algorithms for the verification of temporal properties -- A unified approach to the deadlock detection problem in networks of communicating finite state machines -- Branching time regular temporal logic for model checking with linear time complexity -- The algebraic feedback product of automata -- Synthesizing processes and schedulers from temporal specifications -- Task-driven supervisory control of discrete event systems -- A proof lattice-based technique for analyzing liveness of resource controllers -- Verification of a multiprocessor cache protocol using simulation relations and higher-order logic (summary) -- Computer assistance for program refinement -- Program verification by symbolic execution of hyperfinite ideal machines -- Extension of the Karp and miller procedure to lotos specifications -- An algebra for delay-insensitive circuits -- Finiteness conditions and structural construction of automata for all process algebras -- On automatically explaining bisimulation inequivalence.

Sommario/riassunto

This volume contains the proceedings of the second workshop on Computer Aided Verification, held at DIMACS, Rutgers University, June 18-21, 1990. Itfeatures theoretical results that lead to new or more powerful verification methods. Among these are advances in the use of binary decision diagrams, dense time, reductions based upon partial order representations and proof-checking in controller verification. The motivation for holding a workshop on computer aided verification was to bring together work on effective algorithms or methodologies for formal verification - as distinguished, say,from attributes of logics or formal languages. The considerable interest generated by the first workshop, held in Grenoble, June 1989 (see LNCS 407), prompted this second meeting. The general focus of this volume is on the problem of making formal verification feasible for various models of computation. Specific emphasis is on models associated with distributed programs, protocols, and digital circuits. The general test of algorithm feasibility is to embed it into a verification tool, and exercise that tool on realistic examples: the workshop included sessionsfor the demonstration of new verification tools.