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| 1. | Record Nr. | UNISA996465664503316 |
| | Titolo | Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation [[electronic resource] ] : 19th International Workshop, PATMOS 2009, Delft, The Netherlands, September 9-11, 2009, Revised Selected Papers / / edited by José Monteiro, Rene van Leuken |
| | Pubbl/distr/stampa | Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2010 |
| | ISBN | 1-280-38568-5<br>9786613563606<br>3-642-11802-X |
| | Edizione | [1st ed. 2010.] |
| | Descrizione fisica | 1 online resource (370 p. 234 illus.) |
| | Collana | Theoretical Computer Science and General Issues, , 2512-2029 ; ; 5953 |
| | Classificazione | SS 4800 |
| | Disciplina | 621.39/5 |
| | Soggetti | Computer systems<br>Computer programming<br>Computer engineering<br>Computer networks<br>Microprocessors<br>Computer architecture<br>Computer simulation<br>Computers<br>Computer System Implementation<br>Programming Techniques<br>Computer Engineering and Networks<br>Processor Architectures<br>Computer Modelling<br>Computer Hardware |
| | Lingua di pubblicazione | Inglese |
| | Formato | Materiale a stampa |
| | Livello bibliografico | Monografia |
| | Note generali | Bibliographic Level Mode of Issuance: Monograph |
| | Nota di bibliografia | Includes bibliographical references and index. |
| | Nota di contenuto | Keynotes -- Robust Low Power Embedded SRAM Design: From System to Memory Cell -- Variability in Advanced Nanometer Technologies: Challenges and Solutions -- Subthreshold Circuit Design for Ultra- |

Low-Power Applications -- Special Session -- SystemC AMS Extensions: New Language – New Methods – New Applications -- Session 1: Variability & Statistical Timing -- Process Variation Aware Performance Analysis of Asynchronous Circuits Considering Spatial Correlation -- Interpreting SSTA Results with Correlation -- Residue Arithmetic for Variation-Tolerant Design of Multiply-Add Units -- Exponent Monte Carlo for Quick Statistical Circuit Simulation -- Poster Session 1: Circuit Level Techniques -- Clock Repeater Characterization for Jitter-Aware Clock Tree Synthesis -- A Hardware Implementation of the User-Centric Display Energy Management -- On-chip Thermal Modeling Based on SPICE Simulation -- Switching Noise Optimization in the Wake-Up Phase of Leakage-Aware Power Gating Structures -- Session 2: Power Management -- Application-Specific Temperature Reduction Systematic Methodology for 2D and 3D Networks-on-Chip -- Data-Driven Clock Gating for Digital Filters -- Power Management and Its Impact on Power Supply Noise -- Assertive Dynamic Power Management (AsDPM) Strategy for Globally Scheduled RT Multiprocessor Systems -- Session 3: Low Power Circuits & Technology -- Design Optimization of Low-Power 90nm CMOS SOC Application Using 0.5V Bulk PMOS Dynamic-Threshold with Dual Threshold (MTCMOS): BP-DTMOS-DT Technique -- Crosstalk in High-Performance Asynchronous Designs -- Modeling and Reducing EMI in GALS and Synchronous Systems -- Low-Power Dual-Edge Triggered State Retention Scan Flip-Flop -- Poster Session 2: System Level Techniques -- Multi-granularity NoC Simulation Framework for Early Phase Exploration of SDR Hardware Platforms -- Dynamic Data Type Optimization and Memory Assignment Methodologies -- Accelerating Embedded Software Power Profiling Using Run-Time Power Emulation -- Write Invalidation Analysis in Chip Multiprocessors -- Practical Design Space Exploration of an H264 Decoder for Handheld Devices Using a Virtual Platform -- BSAA: A Switching Activity Analysis and Visualisation Tool for SoC Power Optimisation -- Session 4: Power & Timing Optimization Techniques -- Reducing Timing Overhead in Simultaneously Clock-Gated and Power-Gated Designs by Placement-Aware Clustering -- Low Energy Voltage Dithering in Dual V DD Circuits -- Product On-Chip Process Compensation for Low Power and Yield Enhancement -- Session 5: Self-timed Circuits -- Low-Power Soft Error Hardened Latch -- Digital Timing Slack Monitors and Their Specific Insertion Flow for Adaptive Compensation of Variabilities -- Quasi-Delay-Insensitive Computing Device: Methodological Aspects and Practical Implementation -- The Magic Rule of Tiles: Virtual Delay Insensitivity -- Session 6: Low Power Circuit Analysis & Optimization -- Analysis of Power Consumption Using a New Methodology for the Capacitance Modeling of Complex Logic Gates -- A New Methodology for Power-Aware Transistor Sizing: Free Power Recovery (FPR) -- Routing Resistance Influence in Loading Effect on Leakage Analysis -- Session 7: Low Power Design Studies -- Processor Customization for Software Implementation of the AES Algorithm for Wireless Sensor Networks -- An On-Chip Multi-mode Buck DC-DC Converter for Fine-Grain DVS on a Multi-power Domain SoC Using a 65-nm Standard CMOS Logic Process -- Energy Dissipation Reduction of a Cardiac Event Detector in the Sub-V t Domain By Architectural Folding -- A New Optimized High-Speed Low-Power Data-Driven Dynamic (D3L) 32-Bit Kogge-Stone Adder.

Sommario/riassunto

This book constitutes the thoroughly refereed post-conference proceedings of 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2009, featuring Integrated Circuit and System Design, held in Delft, The Netherlands

during September 9-11, 2009. The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability & statistical timing, circuit level techniques, power management, low power circuits & technology, system level techniques, power & timing optimization techniques, self-timed circuits, low power circuit analysis & optimization, and low power design studies. .

2. Record Nr. UNIORUON00504115

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| Titolo | Manuale di linguistica italiana / a cura di Sergio Lubello |
| Pubbl/distr/stampa | Berlin ; Boston, : De Gruyter, 2016 |
| ISBN | 978-31-10-36085-1 |
| Descrizione fisica | 1 risorsa online (ix, 738 p. ; 23 cm.) |
| Disciplina | 455 |
| Soggetti | Lingua italiana - Aspetti sociali<br>Lingua italiana - Grammatica storica |
| Lingua di pubblicazione | Italiano |
| Formato | Risorsa elettronica |
| Livello bibliografico | Monografia |