1. Record Nr. UNISA996466222103316

Titolo	Automated Technology for Verification and Analysis [[electronic resource]] : Third International Symposium, ATVA 2005, Taipei, Taiwan, October 4-7, 2005, Proceedings / / edited by Doron A. Peled, Yih-Kuen Tsay
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2005
Edizione	[1st ed. 2005.]
Descrizione fisica	1 online resource (XII, 508 p.)
Collana	Programming and Software Engineering ; ; 3707
Disciplina	620.00420285
Soggetti	Computer-aided engineering Computer logic Computer communication systems Special purpose computers Software engineering Programming languages (Electronic computers) Computer-Aided Engineering (CAD, CAE) and Design Logics and Meanings of Programs Computer Communication Networks Special Purpose and Application-Based Systems Software Engineering Programming Languages, Compilers, Interpreters
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Keynote Speeches -- Ranking Abstraction as a Companion to Predicate Abstraction -- Termination and Invariance Analysis of Loops -- Some Perspectives of Infinite-State Verification -- Model Checking -- Verifying Very Large Industrial Circuits Using 100 Processes and Beyond -- A New Reachability Algorithm for Symmetric Multi-processor Architecture -- Comprehensive Verification Framework for Dependability of Self-optimizing Systems -- Exploiting Hub States in Automatic Verification -- Combined Methods -- An Approach for the

Verification of SystemC Designs Using AsmL -- Decomposition-Based Verification of Cyclic Workflows -- Timed, Embedded, and Hybrid Systems (I) -- Guaranteed Termination in the Verification of LTL Properties of Non-linear Robust Discrete Time Hybrid Systems -- Computation Platform for Automatic Analysis of Embedded Software Systems Using Model Based Approach -- Quantitative and Qualitative Analysis of Temporal Aspects of Complex Activities -- Automatic Test Case Generation with Region-Related Coverage Annotations for Real-Time Systems -- Abstraction and Reduction Techniques -- Selective Search in Bounded Model Checking of Reachability Properties -- Predicate Abstraction of RTL Verilog Descriptions Using Constraint Logic Programming -- State Space Exploration of Object-Based Systems Using Equivalence Reduction and the Sweepline Method -- Syntactical Colored Petri Nets Reductions -- Decidability and Complexity -- Algorithmic Algebraic Model Checking II: Decidability of Semi-algebraic Model Checking and Its Applications to Systems Biology -- A Static Analysis Using Tree Automata for XML Access Control -- Reasoning About Transfinite Sequences -- Semi-automatic Distributed Synthesis -- Established Formalisms and Standards -- A New Graph of Classes for the Preservation of Quantitative Temporal Constraints -- Comparison of Different Semantics for Time Petri Nets -- Introducing Dynamic Properties with Past Temporal Operators in the B Refinement -- Approximate Reachability for Dead Code Elimination in Esterel??? -- Compositional Verification and Games -- Synthesis of Interface Automata -- Multi-valued Model Checking Games -- Timed, Embedded, and Hybrid Systems (II) -- Model Checking Prioritized Timed Automata -- An MTBDD-Based Implementation of Forward Reachability for Probabilistic Timed Automata -- Protocols Analysis, Case Studies, and Tools -- An EFSM-Based Intrusion Detection System for Ad Hoc Networks -- Modeling and Verification of a Telecommunication Application Using Live Sequence Charts and the Play-Engine Tool -- Formal Construction and Verification of Home Service Robots: A Case Study -- Model Checking Real Time Java Using Java PathFinder -- Infinite-State and Parameterized Systems -- Using Parametric Automata for the Verification of the Stop-and-Wait Class of Protocols -- Flat Acceleration in Symbolic Model Checking -- Flat Counter Automata Almost Everywhere!.

Sommario/riassunto

The Automated Technology for Veri?cation and Analysis (ATVA) international symposium series was initiated in 2003, responding to a growing interest in formal veri?cation spurred by the booming IT industry, particularly hardware design and manufacturing in East Asia. Its purpose is to promote research on automated veri?cation and analysis in the region by providing a forum for int- action between the regional and the international research/industrial commu- ties of the ? eld. ATVA 2005, the third of the ATVA series, was held in Taipei, Taiwan, October 4–7, 2005. The main theme of the symposium encompasses - sign, complexities, tools, and applications of automated methods for veri?cation and analysis. The symposium was co-located and had a two-day overlap with FORTE 2005, which was held October 2–5, 2005. We received a total of 95 submissions from 17 countries. Each submission was assigned to three Program Committee members, who were helped by their subreviewers, for rigorous and fair evaluation. The ?nal deliberation by the P- gram Committee was conducted over email for a duration of about 10 days after nearly all review reports had been collected. In the end, 33 papers were - lectedforinclusionintheprogram.
ATVA2005hadthreekeynotespeechesgiven respectively by Amir Pnueli (joint with FORTE 2005), Zohar Manna, and Wo- gang Thomas. The

main symposium was preceded by a tutorial day, consisting of three two-hour lectures given also by the keynote speakers.

2. Record Nr. UNIORUON00231559

Autore	MEL'UK, Igor' A.
Titolo	Russkij jazyk v modeli "smysl - tekst" = The Russian language in the meaning - text perspective / I. A. Mel'uk
Pubbl/distr/stampa	Moskva ; Vena, : Jazyki Russkoj kulturj, 1995
ISBN	58-87660-44-9
Descrizione fisica	682 p. ; 23 cm.
Disciplina	491.7
Soggetti	Lingua russa
Lingua di pubblicazione	Russo Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia