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1.9.7 Power Supply (Ground Rail) Undershoot Initiated Latchup1.10 ELECTROSTATIC DISCHARGE SOURCES; 1.10.1 Human Body Model ESD Event; 1.10.2 Machine Model ESD Event; 1.10.3 Cable Discharge Event Source; 1.11 SINGLE EVENT LATCHUP; 1.11.1 High-Energy Photon Emissions; 1.11.2 Alpha Particle Ionizing Source; 1.11.3 Cosmic Ray Source; 1.11.4 Heavy Ion Source; 1.12 SUMMARY AND CLOSING COMMENTS; PROBLEMS; REFERENCES; 2 Bipolar Transistors; 2.1 THE BIPOLAR TRANSISTOR AND CMOS LATCHUP; 2.1.1 Fundamental Equations of Semiconductors and the Drift-Diffusion Current Constitutive Relationships
2.1.2 Diode Forward Bias Conditions2.1.3 Diode Forward Bias Conditions and High-level Injection; 2.2 BIPOLAR TRANSISTOR; 2.2.1 Bipolar Current Gain; 2.2.2 Bipolar Collector-to-Emitter Transport Factor; 2.2.3 Bipolar Current Characteristics; 2.2.4 Bipolar Model Gummel Plot; 2.2.5 Bipolar Current Model-Ebers-Moll Model; 2.2.6 Bipolar Transistor Base Defect; 2.2.7 Bipolar Transistor Emitter Defect; 2.2.8 Bipolar Base Current - Base Defect and Emitter Defect Relation to Bipolar Current Gain; 2.3 RECOMBINATION MECHANISMS; 2.3.1 Shockley-Read-Hall (SRH) Generation-Recombination Model
2.3.2 Auger Recombination Model2.3.3 Surface Recombination Mechanisms; 2.3.4 Surface Recombination Velocity; 2.3.5 Recombination Mechanisms and Neutron Irradiation; 2.3.6 Recombination Mechanisms and Gold Recombination Centers; 2.4 PHOTON CURRENTS IN METALLURGICAL JUNCTIONS; 2.5 AVALANCHE BREAKDOWN; 2.5.1 Bipolar Transistor Breakdown; 2.5.2 MOSFET Avalanche Breakdown; 2.6 VERTICAL BIPOLAR TRANSISTOR MODEL; 2.7 LATERAL BIPOLAR TRANSISTOR MODELS; 2.7.1 Lindmayer-Schneider Model; 2.7.2 Bipolar Current Gain with Lateral and Vertical Contributions
2.7.3 Lateral Bipolar Transistor Models - Nonfield-Assisted

Sommario/riassunto

Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration. Clear methodologies that grant protection from latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand. This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cabl

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