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| Nota di contenuto | RapidIO® The Embedded System Interconnect; Contents; Preface; 1 The Interconnect Problem; 1.1 Processor Performance and Bandwidth Growth; 1.2 Multiprocessing; 1.3 System of Systems; 1.4 Problems with Traditional Buses; 1.4.1 Bus Loading; 1.4.2 Signal Skew; 1.4.3 Expense of Wider Buses; 1.4.4 Problems with PCI; 1.5 The Market Problem; 1.6 RapidIO: A New Approach; 1.6.1 Why RapidIO?; 1.7 Where Will it be Used?; 1.8 An Analogy; References; 2 RapidIO Technology; 2.1 Philosophy; 2.2 The Specification Hierarchy; 2.3 RapidIO Protocol Overview; 2.3.1 Packets and Control Symbols; 2.4 Packet Format 2.5 Transaction Formats and Types2.6 Message Passing; 2.7 Globally Shared Memory; 2.8 Future Extensions; 2.9 Flow Control; 2.9.1 Link Level Flow Control; 2.9.2 End-to-end Flow Control; 2.10 The Parallel Physical Layer; 2.10.1 Parallel Electrical Interface; 2.11 The Serial Physical Layer; 2.11.1 PCS and PMA Layers; 2.11.2 Electrical Interface; 2.12 Link Protocol; 2.13 Maintenance and Error Management; 2.13.1 Maintenance; 2.13.2 System Discovery; 2.13.3 Error Coverage; 2.13.4 |

Error Recovery; 2.14 Performance; 2.14.1 Packet Structures; 2.14.2 Source Routing and Concurrency
2.14.3 Packet Overhead2.15 Operation Latency; References; 3 Devices, Switches, Transactions and Operations; 3.1 Processing Element Models; 3.1.1 Integrated Processor-memory Processing Element Model; 3.1.2 Memory-only Processing Element Model; 3.2 I/O Processing Element; 3.3 Switch Processing Element; 3.4 Operations and Transactions; 3.4.1 Operation Ordering; 3.4.2 Transaction Delivery; 3.4.3 Ordered Delivery System Issues; 3.4.4 Deadlock Considerations; 4 I/O Logical Operations; 4.1 Introduction; 4.2 Request Class Transactions; 4.2.1 Field Definitions for Request Class Transactions
4.3 Response Class Transactions4.3.1 Field Definitions for Response Packet Formats; 4.4 A Sample Read Operation; 4.5 Write Operations; 4.6 Streaming Writes; 4.7 Atomic Operations; 4.8 Maintenance Operations; 4.9 Data Alignment; 5 Messaging Operations; 5.1 Introduction; 5.2 Message Transactions; 5.2.1 Type 10 Packet Format (Doorbell Class); 5.2.2 Type 11 Packet Format (Message Class); 5.2.3 Response Transactions; 5.3 Mailbox Structures; 5.3.1 A Simple Inbox; 5.3.2 An Extended Inbox; 5.3.3 Receiving Messages; 5.4 Outbound Mailbox Structures; 5.4.1 A Simple Outbox; 5.4.2 An Extended Outbox 5.4.3 Transmitting Messages6 System Level Addressing in RapidIO Systems; 6.1 System Topology; 6.2 Switch-based Systems; 6.3 System Packet Routing; 6.4 Field Alignment and Definition; 6.5 Routing Maintenance Packets; 7 The Serial Physical Layer; 7.1 Packets; 7.1.1 Packet Format; 7.1.2 Packet Protection; 7.1.2.1 Packet CRC Operation; 7.1.2.2 16-Bit Packet CRC Code; 7.2 Control Symbols; 7.2.1 Stype0 Control Symbol Definitions; 7.2.1.1 Packet-accepted Control Symbol; 7.2.1.2 Packet-retry Control Symbol; 7.2.1.3 Packet-not-accepted Control Symbol; 7.2.1.4 Status Control Symbol
7.2.1.5 Link-response Control Symbol

Sommario/riassunto

RapidIO - The Embedded System Interconnect brings together one essential volume on RapidIO interconnect technology, providing a major reference work for the evaluation and understanding of RapidIO. Covering essential aspects of the specification, it also answers most usage questions from both hardware and software engineers. It will also serve as a companion text to the specifications when developing or working with the RapidIO interconnect technology. Including the history of RapidIO and case of studies of RapidIO deployment, this really is the definitive reference guide for this new area of