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Mobility; 2.5.1 Vertical Field Dependence; 2.5.2 Lateral Field Dependence; 2.6 Floating Body Effects; 2.6.1 Strong Inversion Kink Effects; 2.6.2 Body Contact; 2.6.3 Various Techniques to Reduce Kink Effects; 2.7 Subthreshold Behavior; 2.7.1 FD versus PD; 2.7.2 PD; 2.7.3 DIBL Dependence; 2.7.4 Latch/GIDL Behavior; 2.8 Impact Ionization; 2.8.1 Basic Analysis; 2.8.2 Body Current; 2.8.3 Monitoring Techniques; 2.9 Breakdown; 2.9.1 Structure Dependence; 2.9.2 Bipolar Induced Effects; 2.9.3 LDD; 2.10 Transient-Induced Leakage; 2.11 History Effects; 2.12 Self-Heating; 2.12.1 Drain Current; 2.12.2 Thermal Resistance; 2.12.3 Thermal Coupling; 2.12.4 AC Behavior; 2.13 Transient Behaviors; 2.13.1 Floating-Body Induced; 2.13.2 History Effect; 2.14 Summary; References; Problems; 3 SOI CMOS Devices-Part II; 3.1 Hot Carriers; 3.1.1 NMOS; 3.1.2 PMOS; 3.1.3 Substrate Current; 3.1.4 Back Gate Bias; 3.1.5 Device Structure Dependence; 3.1.6 Stress Time; 3.1.7 Isolation Structure; 3.1.8 SOI Wafers; 3.1.9 Lifetime; 3.2 Accumulation-Mode Devices; 3.2.1 DC Behavior; 3.2.2 AC Behavior; 3.2.3 Thin-Film Thickness; 3.2.4 Accumulation versus Inversion; 3.3 Double Gate; 3.4 DTMOS; 3.4.1 Basic Performance; 3.4.2 Second-Order Effects; 3.5 Scaling Trends; 3.6 Single Electron Transistors (SET); 3.7 Electrostatic Discharge (ESD); 3.8 Temperature Dependence; 3.8.1 Noise; 3.9 Sensitivity; 3.10 Radiation Effects; 3.11 Summary; References; Problems; 4 Fundamentals of SOI CMOS Circuits; 4.1 Basic Circuit Issues; 4.1.1 Layout; 4.1.2 High Speed and Low Power; 4.1.3 Floating Body; 4.1.4 Self-Heating; 4.2 Floating Body Effects; 4.2.1 Static Logic Circuits; 4.2.2 Pass Gate Transistors; 4.2.3 Switch Network Logic (SNL); 4.2.4 Hysteresis; 4.2.5 Analog Circuits; 4.3 Low-Voltage Circuit Techniques; 4.3.1 Low-Voltage Technology; 4.3.2 Dynamic Body Control; 4.3.3 Sense Amp; 4.4 DTMOS Circuits; 4.4.1 DTMOS Device; 4.4.2 DTMOS Inverter; 4.4.3 DTMOS Buffer; 4.4.4 Advanced DTMOS Devices; 4.4.5 Active Body Control; 4.5 MTCMOS Circuits; 4.6 Noise; 4.7 Self-Heating; 4.8 ESD Circuits; 4.9 System-on-a Chip (SOC) Technology; 4.10 Summary; References; Problems; 5 SOI CMOS Digital Circuits; 5.1 Static Logic Circuits; 5.1.1 SOI CPL; 5.1.2 DTPT; 5.1.3 SOI CVSL; 5.1.4 SOI Adiabatic CVSL; 5.2 Dynamic Logic Circuits; 5.2.1 SOI DTMOS Dynamic Logic Circuit

Sommario/riassunto

A practical, comprehensive survey of SOI CMOS devices and circuits for microelectronics engineers. The microelectronics industry is becoming increasingly dependent on SOI CMOS VLSI devices and circuits. This book is the first to address this important topic with a practical focus on devices and circuits. It provides an up-to-date survey of the current knowledge regarding SOI device behaviors and describes state-of-the-art low-voltage CMOS VLSI analog and digital circuit techniques. Low-Voltage SOI CMOS VLSI Devices and Circuits covers the entire field, from basic concepts to the most advanced