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Titolo	RTL hardware design using VHDL : coding for efficiency, portability, and scalability / / Pong P. Chu
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Edizione	[[First edition].]
Descrizione fisica	1 online resource (695 p.)
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Soggetti	Digital electronics - Data processing VHDL (Computer hardware description language)
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Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references (p. 665-666) and index.
Nota di contenuto	Introduction to digital system design -- Overview of hardware description languages -- Basic language constructs of VHDL -- Concurrent signal assignment statements of VHDL -- Sequential statements of VHDL -- Synthesis of VHDL code -- Combinational circuit design : practice -- Sequential circuit design : principle -- Sequential circuit design : practice -- Finite state machine : principle and practice -- Register transfer methodology : principle -- Register transfer methodology : practice -- Hierarchical design in VHDL -- Parameterized design : principle -- Parameterized design : practice -- Clock and synchronization : principle and practice.
Sommario/riassunto	The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient, portable, and scalable Register Transfer Level (RTL) digital circuits using the

VHDL hardware description language and synthesis software. Focusing on the module-level design, which is composed of functional units, routing circuit, and storage, the book illustrates the relationship between the VHDL constructs and the underlying hardware components, and shows how to develop codes that faithfully reflect the module-level design and can be synthesized into efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDL constructs and hardware components * Conceptual diagrams that illustrate the realization of VHDL codes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce design concepts, procedures, and techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs and coding * One chapter covering the synchronization and interface between multiple clock domains Although the focus of the book is RTL synthesis, it also examines the synthesis task from the perspective of the overall development process. Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation, verification, and testing needs, and can be easily incorporated into a larger system or reused. Discussion is independent of technology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practical examples, this is an excellent textbook for upper-level undergraduate or graduate courses in advanced digital logic. Engineers who need to make effective use of today's synthesis software and FPGA devices should also refer to this book.