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Sommario/riassunto	In the contemporary technology landscape dominated by digital-centric systems and applications, the significance of analog front-end signal

processing remains indispensable. The precision and performance of critical analog, mixed-signal or mm-wave components such as low-noise amplifiers, equalizers, and data converters are fundamentally determined by technological parameters, such as transconductance, DC gain, device matching, linearity, and timing accuracy, among others. Enhancing these parameters through intrinsic design improvements presents a significant challenge and becomes infeasible beyond certain limits with state-of-the-art circuit design techniques. As the performance of CMOS transistors is fundamentally constrained, foreground or background calibration schemes are commonly employed to mitigate the limitations of MOS devices. However, these constraints can be effectively addressed through the implementation of active and passive bulk-driven circuits enabled by silicon-on-insulator (SOI) CMOS technologies. Fully-Depleted Silicon-on-Insulator (FD-SOI) CMOS technologies offer superior transistor characteristics compared to standard bulk CMOS technology, providing enhanced electrical performance, improved power efficiency, and better scalability. This book offers a comprehensive analysis of FD-SOI CMOS technology, presenting key innovations in design methodologies and circuit implementations adopting bulk-biasing techniques across analog, digital, mixed-signal, and mmWave circuits and systems. It addresses critical transistor limitations, including finite transistor gain, offset, mismatch, noise and linearity, among others. The authors provide detailed technical insights, mathematical modelling, design approaches and circuit realizations covering circuit advances using both static and dynamic transistor body-biasing techniques. Emphasis is placed on overcoming state-of-the-art circuit limitations such as finite DC gain, bandwidth, matching/accuracy and power efficiency. These performance metrics are rigorously investigated through mathematical modelling, validated through simulation and experimentally demonstrated using both dynamic and static body-biasing architectures. An essential guide for innovations using dynamic and static transistor body-biasing techniques; Describes FD-SOI CMOS bulk physics incl. the impact on technology parameters; Presents advanced active and passive body-biasing design methods.