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Nota di contenuto	Front Cover; FPGAs: Instant Access; Copyright Page; Contents; About the Author; Chapter 1. The Fundamentals; Why Use FPGAs?; Applications; Some Technology Background; Fusible-link Technology; FPGA Programming Technologies; Instant Summary; Chapter 2. FPGA Architectures; More on Programming Technologies; SRAM-based Devices; Antifuse-based Devices; E ^{sup(2)} PROM/FLASH-based Devices; Hybrid FLASH-SRAM Devices; Fine-, Medium-, and Coarse-grained Architectures; Logic Blocks; MUX-based; LUT-based; LUT versus Distributed RAM versus SR; CLBs versus LABs versus Slices; Logic Cells/Logic Elements Slicing and DicingCLBs and LABs; Distributed RAMs and Shift Registers; Embedded RAMs; Embedded Multipliers, Adders, etc.; Embedded Processor Cores; Hard Microprocessor Cores; Soft Microprocessor Cores; Clock Managers; Clock Trees; Clock Managers; General-purpose I/O; Configurable I/O Standards; Configurable I/O Impedances; Core versus I/O Supply Voltages; Gigabit Transceivers; Multiple Standards; Intellectual Property (IP); Handcrafted IP; IP Core Generators; System Gates versus Real Gates; Instant Summary; Chapter 3. Programming (Configuring) an FPGA; Configuration Cells

Antifuse-based FPGAs; SRAM-based FPGAs; Programming Embedded (Block) RAMs, Distributed RAMs, etc.; Multiple Programming Chains; Quickly Reinitializing the Device; Using the Configuration Port; Serial Load with FPGA as Master; Parallel Load with FPGA as Master; Parallel Load with FPGA as Slave; Serial Load with FPGA as Slave; Using the JTAG Port; Using an Embedded Processor; Instant Summary; Chapter 4. FPGA vs. ASIC Designs; When You Switch from ASIC to FPGA Design, or Vice Versa; Coding Styles; Pipelining and Levels of Logic; Levels of Logic; Asynchronous Design Practices

Asynchronous Structures; Combinational Loops; Delay Chains; Clock Considerations; Clock Domains; Clock Balancing; Clock Gating versus Clock Enabling; PLLs and Clock Conditioning Circuitry; Reliable Data Transfer across Multiclock Domains; Register and Latch Considerations; Latches; Flip-flops with both "Set" and "Reset" Inputs; Global Resets and Initial Conditions; Resource Sharing (Time-Division Multiplexing); Use It or Lose It!; But Wait, There's More; State Machine Encoding; Test Methodologies; Migrating ASIC Designs to FPGAs and Vice Versa; Alternative Design Scenarios; Instant Summary

Chapter 5. ""Traditional"" Design Flows; Schematic-based Design Flows; Back-end Tools like Layout; CAE + CAD = EDA; A Simple (early) Schematic-driven ASIC Flow; A Simple (early) Schematic-driven FPGA Flow; Flat versus Hierarchical Schematics; Schematic-driven FPGA Design Flows Today; HDL-based Design Flows; Advent of HDL-based Flows; A Plethora of HDLs; Points to Ponder; Instant Summary; Chapter 6. Other Design Flows; C/C++-based Design Flows; C versus C++ and Concurrent versus Sequential; SystemC-based Flows; Augmented C/C++-based Flows; Pure C/C++ -based Flows

Different Levels of Synthesis Abstraction

Sommario/riassunto

FPGAs are central to electronic design! The engineers designing these devices are in need of essential information at a moment's notice. The Instant Access Series provides all the critical content that a computer design engineer needs in his or her daily work. This book provides an introduction to FPGAs as well as succinct overviews of fundamental concepts and basic programming. FPGAs are a customizable chip flexible enough to be deployed in a wide range of products and applications. There are several basic design flows detailed including ones based in C/C++, DSP, and HDL. This book is
