

1. Record Nr.	UNINA9911006806203321
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Titolo	Nanoscale MOS transistors : semi-classical transport and applications / / David Esseni, Pierpaolo Palestri, and Luca Selmi
Pubbl/distr/stampa	Cambridge ; ; New York, : Cambridge University Press, 2011
ISBN	1-107-21590-0 1-282-97823-3 9786612978234 0-511-93186-7 0-511-97385-3 0-511-92375-9 0-511-93322-3 0-511-92801-7 0-511-92548-4 0-511-93052-6
Descrizione fisica	1 online resource (xvii, 470 pages) : digital, PDF file(s)
Classificazione	TEC008080
Altri autori (Persone)	PalestriP (Pierpaolo) SelmiL (Luca)
Disciplina	004.5/3
Soggetti	Metal oxide semiconductors - Design and construction Electron transport Nanoelectronics
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Title from publisher's bibliographic system (viewed on 05 Oct 2015).
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Machine generated contents note: 1. Introduction; 2. Bulk semiconductors and the semi-classical model; 3. Quantum confined inversion layers; 4. Carrier scattering in silicon MOS transistors; 5. The Boltzmann transport equation; 6. The Monte Carlo method for the Boltzmann transport equation; 7. Simulation of bulk and SOI silicon MOSFETs; 8. MOS transistors with arbitrary crystal orientation; 9. MOS transistors with strained silicon channels; 10. MOS transistors with alternative materials; Appendix A. Mathematical definitions and properties; Appendix B. Integrals and transformations over a finite area A; Appendix C. Calculation of the equi-energy lines with the k-p

model; Appendix D. Matrix elements beyond the envelope function approximation; Appendix E. Charge density produced by a perturbation potential.

Sommario/riassunto

"Written from an engineering standpoint, this book provides the theoretical background and physical insight needed to understand new and future developments in the modeling and design of n- and p-MOS nanoscale transistors. A wealth of applications, illustrations and examples connect the methods described to all the latest issues in nanoscale MOSFET design. Key areas covered include: Transport in arbitrary crystal orientations and strain conditions, and new channel and gate stack materials All the relevant transport regimes, ranging from low field mobility to quasi-ballistic transport, described using a single modeling framework Predictive capabilities of device models, discussed with systematic comparisons to experimental results"--

"The traditional geometrical scaling of the CMOS technologies has recently evolved in a generalized scaling scenario where material innovations for different intrinsic regions of MOS transistors as well as new device architectures are considered as the main routes toward further performance improvements. In this regard, high- κ dielectrics are used to reduce the gate leakage with respect to the SiO_2 for a given drive capacitance, while the on-current of the MOS transistors is improved by using strained silicon and possibly with the introduction of alternative channel materials. Moreover, the ultra-thin body Silicon-On-Insulator (SOI) device architecture shows an excellent scalability even with a very lightly doped silicon film, while non-planar FinFETs are also of particular interest, because they are a viable way to obtain double-gate SOI MOSFETs and to realize in the same fabrication process n-MOS and p-MOS devices with different crystal orientations"

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