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Nota di contenuto	List of figures; List of tables; Preface; 1. Introduction; 2. Projection-based model order reduction algorithms; 3. Truncated balanced realization methods for model order reduction; 4. Passive balanced truncation of linear systems in descriptor form; 5. Passive hierarchical model order reduction; 6. Terminal reduction of linear dynamic circuits; 7. Vector potential equivalent circuit for inductance modeling; 8. Structure-preserving model order reduction; 9. Block structure-preserving reduction for RLCK circuits; 10. Model optimization and passivity enforcement; 11. General multi-port circuit realization; 12. Model order reduction for multi-terminal linear dynamic circuits; 13. Passive modeling by signal waveform shaping; References; Index.
Sommario/riassunto	Model order reduction (MOR) techniques reduce the complexity of VLSI designs, paving the way to higher operating speeds and smaller feature

sizes. This 2007 book presents a systematic introduction to, and treatment of, the key MOR methods employed in general linear circuits, using real-world examples to illustrate the advantages and disadvantages of each algorithm. Following a review of traditional projection-based techniques, coverage progresses to more advanced MOR methods for VLSI design, including HMOR, passive truncated balanced realization (TBR) methods, efficient inductance modeling via the VPEC model, and structure-preserving MOR techniques. Where possible, numerical methods are approached from the CAD engineer's perspective, avoiding complex mathematics and allowing the reader to take on real design problems and develop more effective tools. With practical examples and over 100 illustrations, this book is suitable for researchers and graduate students of electrical and computer engineering, as well as practitioners working in the VLSI design industry.