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Nota di contenuto	Cover; Half-title; Title; Copyright; Contents; Preface; 1 Controlling complexity; 2 A Verilogical place to start; 3 Defining the instruction set architecture; 4 Algorithmic behavioral modeling; 5 Building an assembler for VeSPA; 6 Pipelining; 7 Implementation of the pipelined processor; 8 Verification; APPENDIX A The VeSPA instruction set architecture (ISA); APPENDIX B The VASM assembler; Index
Sommario/riassunto	This book serves both as an introduction to computer architecture and as a guide to using a hardware description language (HDL) to design, model and simulate real digital systems. The book starts with an introduction to Verilog - the HDL chosen for the book since it is widely used in industry and straightforward to learn. Next, the instruction set architecture (ISA) for the simple VeSPA (Very Small Processor

Architecture) processor is defined - this is a real working device that has been built and tested at the University of Minnesota by the authors. The VeSPA ISA is used throughout the remainder of the book to demonstrate how behavioural and structural models can be developed and intermingled in Verilog. Although Verilog is used throughout, the lessons learned will be equally applicable to other HDLs. Written for senior and graduate students, this book is also an ideal introduction to Verilog for practising engineers.