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| Descrizione fisica | 1 online resource (524 p.) |
| Collana | Advanced Materials Series |
| Disciplina | 615.954 |
| Soggetti | Food contamination Biomedical materials Microbial ecology |
| Lingua di pubblicazione | Inglese |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| Note generali | Description based upon print version of record. |
| Nota di bibliografia | Includes bibliographical references at the end of each chapters and index. |
| Nota di contenuto | Layered double hydroxides and the environment : an overview / Amita Jaiswal, Ravindra Kumar Gautam, and Mahesh Chandra Chattopadhyaya -- Improvement of the corrosion resistance of aluminium alloys applying different types of silanes / Anca-Iulia Stoica, Norica Carmen Godja, Andje Stankovi, Matthias Pilzler, Erich Kny, and Christoph Kleber -- New generation material for the removal of arsenic from water / Dinesh Kumar and Vaishali Tomar -- Prediction and optimization of heavy clay products quality / Milica Arsenovi, Lato Pezo, Lidija Mani, and Zagorka Radojevi -- Enhancement of physical and mechanical properties of sugar palm fiber via vacuum resin impregnation / M.R. Ishak, Z. Leman, S.M. Sapuan, M.Z.A. Rahman, and U.M.K. Anwar -- Environmentally-friendly acrylates-based polymer latices / Sweta Shukla and J.S.P. Rai -- Nanoparticles for trace analysis of toxins : present and future scenario / Anupreet Kaur and Shivender Singh Saini -- Recent developments in gold nanomaterial catalysts for oxidation reaction through green and sustainable routes / Biswajit Chowdhury, Chiranjit Santra, Sandip Mandal, and Rawesh Kumar -- Nanosized |

metal oxide-based adsorbents for heavy metal removal : a review / Deepak Pathania and Pardeep Singh -- Future prospects of phytosynthesized transition metal nanoparticles as novel functional agents for textiles / Shahid-ul-Islam, Mohammad Shahid, and Fageer Mohammad -- Functionalized magnetic nanoparticles for heavy metal removal from aqueous solutions : kinetics and equilibrium modeling / Ravindra Kumar Gautam, Amita Jaiswal, and Mahesh Chandra Chattopadhyaya -- Potential application of nanoparticles as antipathogens / Pratima Chauhan, Mini Mishraand, Deepika Gupta -- Gas barrier properties of biopolymer-based nanocomposites : application in food packaging / Sarat Kumar Swain -- Application of zero-valent iron nanoparticles for environmental clean up / Ritu Singh and Virendra Misra -- Typical synthesis and environmental application of novel TiO₂ nanoparticles / Tanmay Kumar Ghorai -- Zinc oxide nanowire films : solution growth, defect states, and electrical conductivity / Ajay Kushwaha and M. Aslam.

Sommario/riassunto

The levels of toxic and microbial contamination in the food and environment are influenced by harvesting or slaughtering technologies and by the processes applied during food manufacture. With current cultivation methods, it is impossible to guarantee the absence of pesticides and pathogenic microorganisms in raw foods, both of plant and animal origin. Widespread and increasing incidence of foodborne diseases and the resulting social and economic impact on the world population have brought food and environmental safety to the forefront of ecological safety and public health concerns. The emer

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| 2. Record Nr. | UNINA9911006603803321 |
| Autore | Swartzlander Earl E., Jr., <1945-> |
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| Pubbl/distr/stampa | Hackensack, New Jersey : , : World Scientific, , 2015 |
| ISBN | 1-68015-847-3 981-4651-14-1 |
| Descrizione fisica | 1 online resource (xvii, 451 p.) : ill |
| Altri autori (Persone) | SwartzlanderEarl E., Jr., <1945-> LemondsCarl E |
| Disciplina | 005.1 |
| Soggetti | Computer programming Floating-point arithmetic Computer arithmetic |
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| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| Nota di bibliografia | Includes bibliographical references and indexes. |
| Nota di contenuto | pt. I. Overview. 1. IEEE standard for floating-point arithmetic -- pt. II. Floating-point addition. 2. Delay-optimized implementation of IEEE floating-point addition / P. M. Seidel and G. Even -- 3. Using the reverse-carry approach for double datapath floating-point addition / J. D. Bruguera and T. Lang -- 4. Reduced latency IEEE floating-point standard adder architectures / A. Beaumont-Smith ... [et al.] -- 5. Leading-zero anticipatory logic for high-speed floating-point addition / H. Suzuki ... [et al.] -- 6. Leading zero anticipation and detection - A comparison of methods / M. Schmookler and K. Nowka -- 7. S/370 sign-magnitude floating-point adder / S. Vassiliadis, D. S. Lemon and M. Putrino -- pt. III. Floating-point multiplication. 8. A quadruple precision and dual double precision floating-point multiplier / A. Akkas and M. J. Schulte -- 9. A dual mode IEEE multiplier / G. Even, S. M. Mueller and P. M. Seidel -- 10. 167 MHz radix-4 floating-point multiplier / R. K. Yu and G. B. Zyner -- pt. IV. Rounding. 11. Rounding algorithms for IEEE multipliers / M. R. Santoro, G. Bewick and M. A. Horowitz -- 12. "Systematic IEEE rounding method for high-speed floating-point multipliers / N. T. Quach, N. Takagi, and M. J. Flynn -- 13. A comparison of three rounding algorithms for IEEE floating-point |

multiplication / G. Even and P. M. Seidel -- 14. Prenormalization rounding in IEEE floating-point operations using a flagged prefix adder / N. Burgess -- pt. V. Fused multiply add. 15. Design of the IBM RISC system/6000 floating-point execution unit / R. K. Montoye, E. Hokenek and S. L. Runyon -- 16. A 17 x 69 bit multiply and add unit with redundant binary feedback and single cycle latency / W. S. Briggs and D. Matula -- 17. Comparison of single- and dual-pass multiply-add fused floating-point units / R. Jessani and M. Putrino -- 18. Floating-point fused multiply-add with reduced latency / T. Lang and J. D. Bruguera -- 19. Floating-point fused multiply-add architectures / E. Quinell, E. E. Swartzlander, Jr. and C. Lemonds -- pt. VI. Floating-point division. 20. Floating-point division and square root algorithms and implementation in the AMD-K7 microprocessor / S. F. Oberman -- 21. High performance floating-point unit with 116 bit wide divider / G. Gerwig ... [et al.] -- 22. High-speed double-precision computation of reciprocal, division, square root, and inverse square root / J. A. Pineiro and J. D. Bruguera -- 23. 167 MHz radix-8 floating-point divide and square root using overlapped radix-2 stages / J. Prabhu and G. Zyner -- 24. Division algorithms and implementations / S. F. Oberman and M. J. Flynn -- 25. Faithful interpolation in reciprocal tables / D. Das Sarma and D. W. Matula -- pt. VII. Elementary functions. 26. Computation of elementary functions on the IBM RISC system/6000 processor / P. W. Markstein -- 27. Accurate and monotone approximations of some transcendental functions / W. Ferguson and T. Brightman -- 28. The K5 transcendental functions / T. Lynch ... [et al.] -- 29. Hardware designs for exactly rounded elementary functions / M. J. Schulte and E. E. Swartzlander, Jr. -- 30. Toward correctly rounded transcendentals / V. Lefevre, J.-M. Muller and A. Tisserand -- 31. Reciprocation, square root, inverse square root and some elementary functions using small multipliers / M. Ercegovic ... [et al.] -- 32. Multipartite table methods / F. Dinechin and A. Tisserand -- pt. VIII. Decimal floating-point arithmetic. 33. A decimal floating-point specification / M. F. Cowlishaw ... [et al.] -- 34. Decimal floating-point: Algorithm for computers / M. F. Cowlishaw -- 35. A software implementation of the IEEE 754R decimal floating-point arithmetic using the binary encoded format / M. Cornea ... [et al.] -- 36. Decimal floating-point multiplication, / M. A. Erle, B. J. Hickmann and M. J. Schulte -- 37. "A survey of hardware designs for decimal arithmetic / L.-K. Wang ... [et al.]

Sommario/riassunto

Computer Arithmetic Volume III is a compilation of key papers in computer arithmetic on floating-point arithmetic and design. The intent is to show progress, evolution, and novelty in the area of floating-point arithmetic. This field has made extraordinary progress since the initial software routines on mainframe computers have evolved into hardware implementations in processors spanning a wide range of performance. Nevertheless, these papers pave the way to the understanding of modern day processors design where computer arithmetic are supported by floating-point units. The goal of Volume III is to collect the defining document for floating-point arithmetic and many of the key papers on the implementation of both binary and decimal floating-point arithmetic into a single volume. Although fewer than forty papers are included, their reference lists will direct the interested reader to other excellent work that could not be included here. Volume III is specifically oriented to the needs of designers and users of both general-purpose computers and special-purpose digital processors. The book should also be useful to systems engineers, computer architects, and logic designers. It is also intended to serve as a primary text for a course on floating-point arithmetic, as well as a supplementary text for courses in digital arithmetic and high-speed

signal processing.
