

1. Record Nr.	UNINA9910895727603321
Titolo	Estatísticas do comércio internacional / / Instituto Nacional de Estatística, Portugal
Pubbl/distr/stampa	Lisboa, : INE, c1995-
Descrizione fisica	1 online resource
Disciplina	382/.09469/00212
Soggetti	Außenhandelsstatistik Portugal Commerce Annuaire Statistiques commerciales Volume du commerce international Periodicals. Statistics. Portugal Commerce Statistics Periodicals Portugal
Lingua di pubblicazione	Portoghese
Formato	Materiale a stampa
Livello bibliografico	Periodico

2. Record Nr.	UNINA9910968241303321
Autore	Ashenden Peter J
Titolo	The designer's guide to VHDL // Peter J. Ashenden
Pubbl/distr/stampa	Amsterdam ; ; Boston, : Morgan Kaufmann Publishers, c2008
ISBN	9786612285127 9781282285125 1282285122 9780080568850 0080568858
Edizione	[3rd ed.]
Descrizione fisica	1 online resource (933 pages)
Collana	The Morgan Kaufmann series in systems on silicon
Disciplina	621.39/2
Soggetti	VHDL (Computer hardware description language) Electronic digital computers - Computer simulation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references (p. 889-890) and index.
Nota di contenuto	Front Cover; The Designer's Guide to VHDL; Copyright Page; Contents; Preface; Chapter 1. Fundamental Concepts; 1.1 Modeling Digital Systems; 1.2 Domains and Levels of Modeling; 1.3 Modeling Languages; 1.4 VHDL Modeling Concepts; 1.5 Learning a New Language: Lexical Elements and Syntax; Exercises; Chapter 2. Scalar Data Types and Operations; 2.1 Constants and Variables; 2.2 Scalar Types; 2.3 Type Classification; 2.4 Attributes of Scalar Types; 2.5 Expressions and Predefined Operations; Exercises; Chapter 3. Sequential Statements; 3.1 If Statements; 3.2 Case Statements; 3.3 Null Statements 3.4 Loop Statements3.5 Assertion and Report Statements; Exercises; Chapter 4. Composite Data Types and Operations; 4.1 Arrays; 4.2 Unconstrained Array Types; 4.3 Array Operations and Referencing; 4.4 Records; Exercises; Chapter 5. Basic Modeling Constructs; 5.1 Entity Declarations and Architecture Bodies; 5.2 Behavioral Descriptions; 5.3 Structural Descriptions; 5.4 Design Processing; Exercises; Chapter 6. Subprograms; 6.1 Procedures; 6.2 Procedure Parameters; 6.3 Concurrent Procedure Call Statements; 6.4 Functions; 6.5 Overloading; 6.6 Visibility of Declarations; Exercises

Chapter 7. Packages and Use Clauses 7.1 Package Declarations; 7.2 Package Bodies; 7.3 Use Clauses; Exercises; Chapter 8. Resolved Signals; 8.1 Basic Resolved Signals; 8.2 Resolved Signals, Ports, and Parameters; Exercises; Chapter 9. Predefined and Standard Packages; 9.1 The Predefined Packages standard and env; 9.2 IEEE Standard Packages; Exercises; Chapter 10 Case Study: A Pipelined Multiplier Accumulator; 10.1 Algorithm Outline; 10.2 A Behavioral Model; 10.3 A Register-Transfer-Level Model; Exercises; Chapter 11. Aliases; 11.1 Aliases for Data Objects; 11.2 Aliases for Non-Data Items Exercises Chapter 12. Generics; 12.1 Generic Constants; 12.2 Generic Types; 12.3 Generic Lists in Packages; 12.4 Generic Lists in Subprograms; 12.5 Generic Subprograms; 12.6 Generic Packages; Exercises; Chapter 13. Components and Configurations; 13.1 Components; 13.2 Configuring Component Instances; 13.3 Configuration Specifications; Exercises; Chapter 14. Generate Statements; 14.1 Generating Iterative Structures; 14.2 Conditionally Generating Structures; 14.3 Configuration of Generate Statements; Exercises; Chapter 15. Access Types; 15.1 Access Types; 15.2 Linked Data Structures 15.3 An Ordered-Dictionary ADT Using Access Types Exercises; Chapter 16. Files and Input/Output; 16.1 Files; 16.2 The Package Textio; Exercises; Chapter 17. Case Study: A Package for Memories; 17.1 The Memories Package; 17.2 Using the Memories Package; Exercises; Chapter 18. Test Bench and Verification Features; 18.1 External Names; 18.2 Force and Release Assignments; 18.3 Embedded PSL in VHDL; Exercises; Chapter 19. Shared Variables and Protected Types; 19.1 Shared Variables and Mutual Exclusion; 19.2 Uninstantiated Methods in Protected Types; Exercises; Chapter 20. Attributes and Groups 20.1 Predefined Attributes

Sommario/riassunto

VHDL, the IEEE standard hardware description language for describing digital electronic systems, has recently been revised. This book has become a standard in the industry for learning the features of VHDL and using it to verify hardware designs. This third edition is the first comprehensive book on the market to address the new features of VHDL-2008.* First comprehensive book on VHDL to incorporate all new features of VHDL-2008, the latest release of the VHDL standard...helps readers get up to speed quickly with new features of the new standard.
* Presents a structured guide to t
