1. Record Nr.   UNINA9910876805703321

   Autore   Voldman Steven H

   Titolo   Latchup / / Steven H. Voldman

   Pubbl/distr/stampa   Chichester, West Sussex, England ; ; Hoboken, NJ, : John Wiley, c2007

   ISBN   1-281-31816-7
                        9786611318161
                        0-470-51617-8
                        0-470-51616-X

   Descrizione fisica   1 online resource (474 p.)

   Disciplina   621.3815/2

   Soggetti   Metal oxide semiconductors, Complementary - Defects
                        Metal oxide semiconductors, Complementary - Reliability

   Lingua di pubblicazione   Inglese

   Formato   Materiale a stampa

   Livello bibliografico   Monografia

   Note generali   Description based upon print version of record.

   Nota di bibliografia   Includes bibliographical references and index.

   Nota di contenuto   Latchup; Contents; About the Author; Preface; Acknowledgements; 1
                        CMOS Latchup; 1.1 CMOS LATCHUP; 1.1.1 CMOS Latchup-What is
                        Latchup?; 1.1.2 CMOS Latchup-Why is Latchup Still an Issue ?; 1.1.3
                        Early CMOS Latchup History; 1.2 FUNDAMENTAL CONCEPTS OF
                        LATCHUP DESIGN PRACTICE; 1.3 BUILDING A CMOS LATCHUP
                        STRATEGY; 1.3.1 Building a CMOS Business Strategy - 18 Steps in
                        Building a CMOS Latchup Business Strategy; 1.3.2 Building a CMOS
                        Latchup Technology Strategy - 18 Steps in Building a CMOS Latchup
                        Technology Strategy; 1.4 CMOS LATCHUP TECHNOLOGY MIGRATION
                        STRATEGY
                        1.5 KEY METRICS OF LATCHUP DESIGN PRACTICE1.6 CMOS LATCHUP
                        TECHNOLOGY TRENDS AND SCALING; 1.7 KEY DEVELOPMENTS; 1.7.1
                        Key Innovations; 1.7.2 Key Contributions; 1.7.3 Key Patents; 1.8
                        LATCHUP FAILURE MECHANISMS; 1.9 CMOS LATCHUP EVENTS; 1.9.1
                        Power-Up Sequence Initiated Latchup; 1.9.2 Input Pin Overshoot and
                        Power-Up Sequence Initiated Latchup; 1.9.3 Input Pin Undershoot and
                        Power-Up Sequence Initiated Latchup; 1.9.4 Multiple Power Supply
                        Power-Up Sequence Initiated Latchup; 1.9.5 Power Supply Overshoot
                        Initiated Latchup; 1.9.6 Power Supply Undershoot Initiated Latchup
                        1.9.7 Power Supply (Ground Rail) Undershoot Initiated Latchup1.10

| Sommario/riassunto | Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration. Clear methodologies that grant protection from latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand. This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cabl |