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Sommario/riassunto	Long description: The aim of this workshop is to make FPGA and reconfigurable technology accessible to software programmers. Despite their frequently proven power and performance benefits, designing for FPGAs is mostly an engineering discipline carried out by highly trained specialists. With recent progress in high-level synthesis, a first important step towards bringing FPGA technology to potentially millions of software developers was taken. The FSP Workshop aims at bringing researchers and experts from both academia and industry together to discuss and exchange the latest research advances and future trends. This includes high-level compilation and languages, design automation tools that raise the abstraction level when designing for (heterogeneous) FPGAs and reconfigurable systems and

standardized target platforms. This will in particular put focus on the requirements of software developers and application engineers. In addition, a distinctive feature of the workshop will be its cross section through all design levels, ranging from programming down to custom hardware. Thus, the workshop is targeting all those who are interested in understanding the big picture and the potential of domain-specific computing and software-driven FPGA development. In addition, the FSP Workshop shall facilitate collaboration of the different domains. Topics of the FSP Workshop include, but are not limited to:

- High-level synthesis (HLS) and domain-specific languages (DSLs) for FPGAs and heterogeneous systems
- Mapping approaches and tools for heterogeneous FPGAs
- Support of hard IP blocks such as embedded processors and memory interfaces
- Development environments for software engineers (automated tool flows, design frameworks and tools, tool interaction)
- FPGA virtualization (design for portability, resource sharing, hardware abstraction)
- Design automation technologies for multi-FPGA and heterogeneous systems
- Methods for leveraging (partial) dynamic reconfiguration to increase performance, flexibility, reliability, or programmability
- Operating system services for FPGA resource management, reliability, security
- Target hardware design platforms (infrastructure, drivers, portable systems)
- Overlays (CGRAs, vector processors, ASIP- and GPU-like intermediate fabrics)
- Applications (e.g., embedded computing, signal processing, bio informatics, big data, database acceleration) using C/C++/SystemC-based HLS, OpenCL, OpenSPL, etc.
- Directions for collaborations (research proposals, networking, Horizon 2020)
