

1. Record Nr.	UNINA9910872648603321
Titolo	Multiple-Valued Logic: ISMVL '98
Pubbl/distr/stampa	[Place of publication not identified], : I E E E Imprint, 1998
Descrizione fisica	1 online resource
Disciplina	511.3
Soggetti	Many-valued logic Switching theory
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Proceedings. 1998 28th IEEE International Symposium on Multiple-Valued Logic (Cat. No.98CB36138) -- Table of contents -- Advanced circuit technology to realize post giga-bit DRAM -- Development of InGaAs-based multiple-junction surface tunnel transistors for multiple-valued logic circuits -- Ultrafast ternary quantizer using resonant tunneling devices -- A Josephson ternary memory circuit -- A note on realizing multiple-valued logic functions using Akers' cells-cell sizes and path lengths -- Minimization of exclusive sums of multi-valued complex terms for logic cell arrays -- Minimal test set generation for fault diagnosis in R-valued PLAs.