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Nota di contenuto	Matching memory to the power of personal computers / R. Foss -- A low-cost, high performance three-dimensional memory module technology / A. Glaser ... [et al.] -- High speed circuit techniques in a 150MHz 64M SDRAM / V. Lines ... [et al.] -- An analysis of (linked) addressed decoder faults / A. van de Goor, G. Gaydadjiev -- SRAM yield estimation in the early stage of the design cycle / V. Kim, T. Chen -- False write through and un-restored write electrical level fault models for SRAMs / R. Adams, E. Cooley -- A defect-tolerant DRAM employing a hierarchical redundancy scheme, built-in self-test and self-reconfiguration / D. Niggemeyer, J. Otterstedt, M. Redeker -- Formal verification of memory arrays using symbolic trajectory evaluation / M. Pandey, R. Bryant -- A product development flow with metrics for memory designs / S. Hegde, I. Pal, K. Rao -- A low-power high storage capacity structure for GaAs MESFET ROM / R. Kanan ... [et al.] -- Use of selective precharge for low-power on the match lines of content-addressable memories / C. Zukowski, S. Wang -- An open notation for memory tests / A. Offerman, A. van de Goor -- Testing memory modules in SRAM-based configurable FPGAs / W. Huang ... [et al.] -- Memory array testing through a scannable configuration / S. Yano, N.

Ishiura -- A high-speed parallel sensing scheme for multi-level non-volatile memories / C. Calligaro ... [et al.]
