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| 1. Record Nr.           | UNINA9910872447003321  |
| Titolo                  | 17th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems (DFT 2002)   |
| Pubbl/distr/stampa      | [Place of publication not identified], : IEEE Computer Society Press, 2002   |
| Descrizione fisica      | 1 online resource (456 pages)  |
| Disciplina              | 621.395  |
| Soggetti                | Integrated circuits - Very large scale integration   |
| Lingua di pubblicazione | Inglese  |
| Formato                 | Materiale a stampa   |
| Livello bibliografico   | Monografia   |
| Note generali           | Bibliographic Level Mode of Issuance: Monograph  |
| Sommario/riassunto      | These 45 papers from the November 2002 symposium discuss techniques to assess and enhance the yield, reliability, and availability of VLSI systems. Several of the contributors present new approaches to fault simulation and injection, concurrent error detection, yield prediction, and sequential circuit design for testability. Specific topics include a simplified gate-level fault model for crosstalk effects analysis, input ordering in concurrent checkers to reduce power consumption, on-chip jitter measurement for phase locked loops, and a method to evaluate the repairability of embedded multiple regions DRAMs. No subject index. Annotation copyrighted by Book News, Inc., Portland, OR. |