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Nota di contenuto	Memory Technology, Design and Testing -- Future trends in flash memories -- Recent developments in dram testing -- Built in self testing for detection of coupling faults in semiconductor memories -- A built in self test scheme for 256Meg sdram -- Proposed on-chip test structure to quantify trap densities within flash meories -- A concurrent placement and routing strategy for improving the quality of application specific memory designs -- Flash memory quality and reliability issues -- A low power current sensing scheme for cmos sram.
Sommario/riassunto	The keynote speech on future trends in flash memories is followed by 16 additional review and research papers. Among the topics are built-in self-testing for detecting of coupling faults in semiconductor memories, a low-power current sensing scheme for CMOS SRAM, scanning capacitance microscopy analysis of DRAM trench capacitors, the thermal monitoring of memories, and a true testprocessor-per-pin algorithmic pattern generator. No subject index. Annotation copyrighted by Book News, Inc., Portland, OR.