

1. Record Nr.	UNINA9910872423203321
Titolo	1997 International Symposium on VLSI Technology, Systems and Applications
Pubbl/distr/stampa	[Place of publication not identified], : IEEE, 1997
Descrizione fisica	1 online resource (xi, 369 pages) : illustrations
Disciplina	621.395
Soggetti	Integrated circuits - Very large scale integration
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	<p>1997 International Symposium on VLSI Technology, Systems, and Applications [front matter] -- Design Issues For Low Power Mobile Transceiver Frontends -- Challenge To The 300mm Technology -- Copper Interconnect: Fabrication And Reliability -- Study Of Integration Issues Of Ti Salicide Process With Preamorphization For Sub-0.18 /spl mu/m Gate Length CMOS Technologies -- Device Degradation Associated With Pre-amorphization Of The Ti Salicide Process -- Electrical Characteristics Of Ti-salicyded N-mosfets With Asymmetric Source/drain Regions -- Challenges And Issues Of Low-k Dielectrics -- Efficient Output ESD Protection Of High-speed Sram Ic With Well-coupled Technique In Sub-pm Cmos Technology -- Advanced Layout Design For Deep-submicron Cmos Output Buffer With Higher Driving Capability And Better ESD Reliability -- Fluorine Penetration Suppression By Applying Amorphous Silicon In Wsi Gate Process -- Image Capture Circuits in CMOS -- A High Resolution Cmos Imager With Active Pixel Using Capacitively Coupled Bipolar Operation -- An Easy-to-design Rail-to-rail CMOS Op Amp With High CMRR -- Area-efficient VDD-to-vSS ESD Clamp Circuit By Using Substrate-triggering Field-oxide Device (STFFOD) For Whole-chip ESD Protection -- Reduction Of Crosstalk In Mixed Signal Integrated Circuits -- A Delayed Synchronizer In High-speed Memory Applications -- A Current-mode Circuit For Euclidean Distance Calculation -- Programmable Media & Graphics Processors -- A Hardware-efficient Architecture For 3-D Graphics Processor -- A High-performance Video Format Conversion</p>

System For MPEG-4 -- A Parallel VLSI Architecture For The LZW Data
Compression Algorithm -- Arc: An Atm Routing And Concentration
Chip.
