

1. Record Nr.	UNINA9910830731003321
Autore	Kilts Steve <1978->
Titolo	Advanced FPGA design : architecture, implementation, and optimization // Steve Kilts
Pubbl/distr/stampa	Hoboken, New Jersey : , : Wiley : , c2007
ISBN	1-280-91682-6 9786610916825 0-470-12789-9 0-470-12788-0
Descrizione fisica	1 online resource (354 p.)
Disciplina	621.395
Soggetti	Field programmable gate arrays - Design and construction
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references (p. 319-320) and index.
Nota di contenuto	Preface -- Acknowledgments -- Chapter 1. Architecting Speed -- High Throughput -- Low Latency -- Timing -- Add Register Layers -- Parallel Structures -- Flatten Logic Structures -- Register Balancing -- Reorder Paths -- Summary of Key Points -- Chapter 2. Architecting Area -- Rolling-up the Pipeline -- Control Based Logic Reuse -- Resource Sharing -- Impact of Reset on Area -- Resources without Reset -- Resources without Set -- Resources without Asynchronous Reset -- Resetting RAM -- Utilizing Set/Reset Flip-Flop Pins -- Summary of Key Points -- Chapter 3. Architecting Power -- Clock Gating -- Clock Skew -- Managing Skew -- Gated Domains -- Input Control -- Reducing the Voltage Supply -- Dual-Edge Triggered Flip-Flops -- Modifying Terminations -- Summary of Key Points -- Chapter 4. Example Design: The Advanced Encryption Standard -- AES Architectures -- Compact Architecture -- Partially Pipelined Architecture -- Fully Pipelined Architecture -- Performance versus Area -- Other Optimizations -- Chapter 5. High Level Design -- Abstract Design Techniques -- Graphical State Machines -- DSP Design -- Software/Hardware Co-Design -- Summary of Key Points -- Chapter 6. Clock Domains -- Crossing Clock Domains -- Metastability -- Solution 1: Phase Control -- Solution 2: Double-flopping -- Solution 3: FIFO Structure -- Partitioning Synchronizer Blocks -- Gated Clocks in ASIC

Prototypes -- Clocks Module -- Gating Removal -- Summary of Key Points -- Chapter 7. Example Design: I2S versus SPDIF -- I2S -- Protocol -- Hardware Architecture -- Analysis -- SPDIF -- Protocol -- Hardware Architecture -- Analysis -- Chapter 8. Implementing Math Functions -- Hardware Division -- Multiply and Shift -- Iterative Division -- The Goldschmidt Method -- Taylor and Maclaurin Series Expansion -- The CORDIC Algorithm -- Summary of Key Points -- Chapter 9. Example Design: Floating Point Unit -- Floating Point Formats -- Pipelined Architecture.

Verilog Implementation -- Resources and Performance -- Chapter 10. Reset Circuits -- Asynchronous versus Synchronous -- Problems with Fully Asynchronous Resets -- Fully Synchronized Resets -- Asynchronous Assertion, Synchronous Deassertion -- Mixing Reset Types -- Non-Resettable Flip-Flops -- Internally Generated Resets -- Multiple Clock Domains -- Summary of Key Points -- Chapter 11. Advanced Simulation -- Testbench Architecture -- Testbench Components -- Testbench Flow -- Main Thread -- Clocks and Resets -- Testcases -- System Stimulus -- Matlab -- Bus-functional Models -- Code Coverage -- Gate Level Simulations -- Toggle Coverage -- Run-Time Traps -- Timescale -- Glitch Rejection -- Combinatorial Delay Modeling -- Summary of Key Points -- Chapter 12. Coding for Synthesis -- Decision Trees -- Priority versus Parallel -- Full Conditions -- Multiple Control Branches -- Traps -- Blocking versus Nonblocking -- For Loops -- Combinatorial Loops -- Inferred Latches -- Functions -- Design Organization -- Partitioning -- Datapath versus Control -- Clock and Reset Structures -- Multiple Instantiations -- Parameterization -- Definitions -- Parameters -- Parameters in Verilog-2001 -- Summary of Key Points -- Chapter 13. Example Design: The Secure Hash Algorithm -- SHA-1 Architecture -- Implementation Results -- Chapter 14. Synthesis Optimization -- Speed versus Area -- Resource Sharing -- Pipelining, Retiming, and Register Balancing -- The Effect of Reset on Register Balancing -- Resynchronization Registers -- FSM Compilation -- Removal of Unreachable States -- Black Boxes -- Physical Synthesis -- Forward versus Back-Annotation -- Graph Based Physical Synthesis -- Summary of Key Points -- Chapter 15. Floorplanning -- Design Partitioning -- Critical Path Floorplanning -- Floorplanning Dangers -- Optimal Floorplanning -- Data Path -- High Fan-Out -- Device Structure -- Reusability -- Reducing Power Dissipation.

Summary of Key Points -- Chapter 16. Place and Route Optimization -- Optimal Constraints -- Relationship between Placement and Routing -- Logic Replication -- Optimization across Hierarchy -- I/O Registers -- Pack Factor -- Mapping Logic into RAM -- Register Ordering -- Placement Seed -- Guided Place and Route -- Summary of Key Points -- Chapter 17. Example Design: Microprocessor -- SRC Architecture -- Synthesis Optimizations -- Speed versus Area -- Pipelining -- Physical Synthesis -- Floorplan Optimizations -- Partitioned Floorplan -- Critical Path Floorplan: Abstraction 1 -- Critical Path Floorplan: Abstraction 2 -- Chapter 18. Static Timing Analysis -- Standard Analysis -- Latches -- Asynchronous Circuits -- Combinatorial Feedback -- Event Driven Clocks -- Summary of Key Points -- Chapter 19. PCB Issues -- Power Supply -- Supply Requirements -- Regulation -- Decoupling Capacitors -- Concept -- Calculating Values -- Capacitor Placement -- Power Planes -- Modeling Signal Reflections -- Spice Simulations -- Configuration -- Debug -- Code Modifications -- FPGA Editor -- Placement -- Properties -- Routing -- ChipScope -- Identify -- Summary of Key Points -- Appendix A -- Appendix B -- Bibliography -- Index.

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real-world experience.
