

- |                         |   |
|-------------------------|---|
| 1. Record Nr.           | UNIPARTHENOPE000012147  |
| Autore                  | Fishburn, Peter C.  |
| Titolo                  | Mathematics of decision theory / by Peter C. Fishburn   |
| Pubbl/distr/stampa      | Paris : Mouton, c1972   |
| Descrizione fisica      | 104 p. ; 23 cm  |
| Collana                 | Methods and models in the social sciences ; 003   |
| Disciplina              | 510   |
| Collocazione            | 510/103   |
| Lingua di pubblicazione | Inglese   |
| Formato                 | Materiale a stampa  |
| Livello bibliografico   | Monografia  |
| 2. Record Nr.           | UNINA9910830451403321   |
| Autore                  | Talbot Daniel (Daniel B.)   |
| Titolo                  | Frequency acquisition techniques for phase locked loop // author Daniel Talbot                                      |
| Pubbl/distr/stampa      | Hoboken, New Jersey : , : John Wiley & Sons, Inc., , [2012]<br>[Piscataway, New Jersey] : , : IEEE Xplore, , [2012] |
| ISBN                    | 1-118-38330-3<br>1-283-59323-8<br>9786613905680<br>1-118-38331-1  |
| Descrizione fisica      | 1 online resource (238 p.)  |
| Disciplina              | 621.3815/486<br>621.382   |
| Soggetti                | Frequency synthesizers<br>Phase-locked loops  |
| Lingua di pubblicazione | Inglese   |
| Formato                 | Materiale a stampa  |
| Livello bibliografico   | Monografia  |
| Note generali           | Description based upon print version of record.   |

Preface xi -- 1 Introduction 1 -- 2 A Review of PLL Fundamentals 3 -- 2.1 What is a PLL?, 3 -- 2.2 Second-Order PLL, 7 -- 2.3 Second-Order PLL Type One, 7 -- 2.4 Second-Order PLL Type Two, 7 -- 2.5 Higher-Order PLL's, 8 -- 2.6 Disturbances, 8 -- 2.7 Frequency Steering and Capture, 9 -- 2.8 Effect of DC Offsets or Noise Prior to the Loop Filter, 10 -- 2.9 Injection-Locked Oscillations, 15 -- 3 Simulating the PLL Linear Operation Mode 17 -- 3.1 Linear Model, 17 -- 3.2 A Word About Damping, 19 -- 4 Sideband Suppression Filtering 21 -- 4.1 Reference Sidebands and VCO Pushing, 21 -- 4.2 Superiority of the Cauer (or Elliptical) Filter, 22 -- 5 Pros and Cons of Sampled Data Phase Detection 25 -- 5.1 What are the Forms of Sampled Data Phase Detectors?, 25 -- 5.2 A. Ramp and Sample Analog Phase Detector, 25 -- 5.3 B. The RF Sampling Phase Detector, 28 -- 5.4 C. Edge-Triggered S-R Flip-Flop, 29 -- 5.5 D. Edge-Triggered Flip-Flop Ensemble, 31 -- 5.6 E. Sample and Hold as a Phase Detector, 31 -- 6 Phase Compression 33 -- 7 Hard Limiting of a Signal Plus Noise 35 -- 8 Phase Noise and Other Spurious Interferers 39 -- 8.1 The Mechanism for Phase Noise in an Oscillator, 42 -- 8.2 Additive Noise in an FM Channel and the Bowtie, 42 -- 8.3 Importance of FM Theory to Frequency Acquisition, 45 -- 9 Impulse Modulation and Noise Aliasing 47 -- 9.1 Impulse Train Spectrum, 47 -- 9.2 Sampling Phase Detector Noise, 47 -- 9.3 Spur Aliasing, 50 -- 10 Time and Phase Jitter, Heterodyning, and Multiplication 53 -- 10.1 Heterodyning and Resulting Time Jitter, 53 -- 10.2 Frequency Multiplication and Angle Modulation Index, 54 -- 10.3 Frequency Multiplication's Role in Carrier Recovery, 54 -- 11 Carrier Recovery Applications and Acquisition 57 -- 11.1 Frequency Multiplier Carrier Recovery in General, 57 -- 11.2 The Simplest Form of Costas PLL, 59 -- 11.3 Higher Level Quadrature Demodulation Costas PLL, 61 -- 11.4 False Lock in BPSK Costas PLL, 62 -- 11.5 Additional Measures for Prevention of False Locking, 65. 11.6 False Lock Prevention Using DC Offset, 72 -- 12 Notes on Sweep Methods 73 -- 12.1 Sweep Waveform Superimposed Directly on VCO Input, 73 -- 12.2 Maximum Sweep Rate (Acceleration), 74 -- 12.3 False Lock due to High-Order Filtering, 77 -- 12.4 Sweep Waveform Applied Directly to PLL Loop Integrator, 79 -- 12.5 Self-Sweeping PLL, 79 -- 13 Nonsweep Acquisition Methods 85 -- 13.1 Delay Line Frequency Discriminator, 85 -- 13.2 The Fully Unbalanced Quadricorrelator, 87 -- 13.3 The Fully Balanced Quadricorrelator, 88 -- 13.4 The Multipulse Balanced Quadricorrelator, 89 -- 13.5 Conclusion Regarding Pulsed Frequency Detection, 91 -- 13.6 Quadricorrelator Linearity, 92 -- 13.7 Limiter Asymmetry due to DC Offset, 97 -- 13.8 Taylor Series Demonstrates Second-Order-Caused DC Offset, 100 -- 13.9 Third-Order Intermodulation Distortion and Taylor Series, 101 -- 14 AM Rejection in Frequency Detection Schemes 105 -- 14.1 AM Rejection with Limiter and Interferer, 105 -- 14.2 AM Rejection of the Balanced Limiter/Quadricorrelator Versus the Limiter/Discriminator in the Presence of a Single Spur, 106 -- 14.3 Impairment due to Filter Response Tilt (Asymmetry), 110 -- 14.4 Bandpass Filter Geometric and Arithmetic Symmetry, 114 -- 14.5 Comments on Degree of Scrutiny, 117 -- 15 Interfacing the Frequency Discriminator to the PLL 119 -- 15.1 Continuous Connection: Pros and Cons, 119 -- 15.2 Connection to PLL via a Dead Band, 120 -- 15.3 Switched Connection, 121 -- 16 Actual Frequency Discriminator Implementations 125 -- 16.1 Quadricorrelator, Low-Frequency Implementation, 125 -- 16.2 Frequency Ratio Calculating Circuit for Wide-Bandwidth Use, 128 -- 16.3 Dividing the Frequency and Resultant Implementation, 131 -- 16.4 Marriage of Both Frequency and Phaselock Loops, 135 -- 16.5

Comments on Spurs' Numerical Influence on the VCO, 141 -- 16.6 Frequency Compression, 143 -- 17 Clock Recovery Using a PLL 145 -- 17.1 PLL Only, 145 -- 17.2 PLL with Sideband Crystal Filter(s), 152 -- 17.3 PLL with Sideband Cavity Filter, 153. 17.4 The Hogge Phase Detector, 161 -- 17.5 Bang-Bang Phase Detectors, 162 -- 18 Frequency Synthesis Applications 165 -- 18.1 Direct Frequency Synthesis with Wadley Loop, 166 -- 18.2 Indirect Frequency Synthesis with PLLs, 173 -- 18.3 Simple Frequency Acquisition Improvement for a PLL, 175 -- 18.4 Hybrid Frequency Synthesis with DDS and PLL, 176 -- 18.5 Phase Noise Considerations, 181 -- 18.6 Pros and Cons of DDS-Augmented Synthesis, 185 -- 18.7 Multiple Loops, 185 -- 18.8 Reference Signal Considerations and Filtering, 186 -- 18.9 SNR of Various Phase Detectors, 187 -- 18.10 Phase Detector Dead Band (Dead Zone) and Remediation, 187 -- 18.11 Sideband Energy due to DC Offset Following Phase Detector, 191 -- 18.12 Brute Force PLL Frequency Acquisition via Speedup, 193 -- 18.13 Short-Term and Long-Term Settling, 193 -- 18.14 N-over-M Synthesis, 193 -- 19 Injection Pulling of Multiple VCO's as in a Serdes 195 -- 19.1 Allowable Coupling Between any Two VCOs Versus Q and BW, 195 -- 19.2 Topology Suggestion for Eliminating the Injection Pulling, 195 -- 20 Digital PLL Example 199 -- 21 Conclusion 203 -- References 205 -- Index 209.

---

## Sommario/riassunto

How to acquire the input frequency from an unlocked state A phase locked loop (PLL) by itself cannot become useful until it has acquired the applied signal's frequency. Often, a PLL will never reach frequency acquisition (capture) without explicit assistive circuits. Curiously, few books on PLLs treat the topic of frequency acquisition in any depth or detail. Frequency Acquisition Techniques for Phase Locked Loops offers a no-nonsense treatment that is equally useful for engineers, technicians, and managers. Since mathematical rigor for its own sake can degenerate into intellectual "rigor mortis," the author introduces readers to the basics and delivers useful information with clear language and minimal mathematics. With most of the approaches having been developed through years of experience, this completely practical guide explores methods for achieving the locked state in a variety of conditions as it examines: Performance limitations of phase/frequency detector-based phase locked loops. The quadricorrelator method for both continuous and sampled modes. Sawtooth ramp-and-sample phase detector and how its waveform contains frequency error information that can be extracted. The benefits of a self-sweeping, self-extinguishing topology. Sweep methods using quadrature mixer-based lock detection. The use of digital implementations versus analog Frequency Acquisition Techniques for Phase Locked Loops is an important resource for RF/microwave engineers, in particular, circuit designers; practicing electronics engineers involved in frequency synthesis, phase locked loops, carrier or clock recovery loops, radio-frequency integrated circuit design, and aerospace electronics; and managers wanting to understand the technology of phase locked loops and frequency acquisition assistance techniques or jitter attenuating loops.

---

3. Record Nr.	UNINA9910165006303321
Autore	Reader Capitol
Titolo	Summary of The Case for Democracy
Pubbl/distr/stampa	Cork, : Primento Digital, 2013
ISBN	9782511001882 2511001888
Descrizione fisica	1 online resource (23 p.)
Disciplina	341.20934589
Soggetti	Democracy Human rights
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di contenuto	Title page; Book Presentation; Book Abstract; About the Author; Important Note About This Ebook; Summary of The Case for Democracy (Natan Sharansky (with Ron Dermer)); From the "Evil Empire" to Perestroika to Freedom; Is Freedom for Everyone?; A Free Society and a Fear Society; Stability Versus Democracy; Mission Possible; Helsinki versus Oslo; Moral Clarity; A Missed Opportunity; Conclusion; Buy the Book; About the Summary Publisher; Copyright
Sommario/riassunto	This ebook consists of a summary of the ideas, viewpoints and facts presented by Nathan Sharansky in his book "The Case for Democracy: The Power of Freedom to Overcome Tyranny and Terror". This summary offers a concise overview of the entire book in less than 30 minutes reading time. However this work does not replace in any case Nathan Sharansky's book. Sharansky argues that human rights and democracy go together, and he also says that promoting peace and stability in the world is equivalent to spreading freedom. Therefore he argues that societies based on fear cannot compete with free societ