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Lithographic Infrastructure; 2.2.3 Immersion Exposure Tools; 2.2.4 Overlay; 2.2.5 Cooptimization of the Mask, the Illuminator, and Apodization; 2.2.6 Optical Proximity Correction; 2.2.7 Double Patterning; 2.2.8 Lithographic Roadmap; 2.3 Lithography Limited Yield 2.3.1 Deviations of Printed Shape from Drawn Polygon2.3.2 Increased Variabilities; 2.3.3 Catastrophic Failures; 2.4 Lithography-Driven DFM Solutions; 2.4.1 Practical Boundary Conditions for DFM; 2.4.2 Classical Approach; 2.4.3 Printability Checkers; 2.4.4 Model-Based Design Rule Checks; 2.4.5 ASIC Cell Optimizations; 2.4.6 Lithography-Aware Routers; 2.4.7 Advanced OPC Techniques for Improved Manufacturing; References; 3 Interaction of Layout with Transistor Performance and Stress Engineering Techniques; 3.1 Introduction; 3.2 Impact of Stress on Transistor Performance; 3.2.1 Electron Mobility
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4.2.1 Process Scaling and Interconnect Fabrication

Sommario/riassunto

Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano-CMOS Design for Manufacturability examines the challenges that design engineers face in the nano-scaled era, such as exacerbated effects and the proven design for manufacturability (DFM) methodology in the midst of increasing variability and design process interactions. In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore's law, the authors also tackle complex issues in the design process to overcome the difficulties, incl