1. Record Nr. UNINA9910829969203321

Titolo	Handbook of 3D integration [[electronic resource]] : technology and applications of 3D integrated circuits / / edited by Philip Garrou, Christopher Bower and Peter Ramm
Pubbl/distr/stampa	Weinheim, : Wiley-VCH, 2008
ISBN	1-283-86967-5 3-527-62306-X 3-527-62305-1
Descrizione fisica	1 online resource (801 p.)
Altri autori (Persone)	GarrouPhilip E BowerChristopher Andrew RammPeter
Disciplina	621.381 621.3815
Soggetti	Integrated circuits Integrated circuits - Design and construction Semiconductor wafers Three-dimensional imaging
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Handbook of 3D Integration; Contents; Preface; List of Contributors; 1 Introduction to 3D Integration; 1.1 Introduction; 1.2 Historical Evolution of Stacked Wafer Concepts; 1.3 3D Packaging vs 3D Integration; 1.4 Non-TSV 3D Stacking Technologies; 1.4.1 Irvine Sensors; 1.4.2 UTCS (Ultrathin Chip Stacking) IMEC, CNRS, U. Barcelona; 1.4.3 Fujitsu; 1.4.4 Fraunhofer/IZM; 1.4.5 3D Plus/Leti; 1.4.6 Toshiba System Block Module; References; 2 Drivers for 3D Integration; 2.1 Introduction; 2.2 Electrical Performance; 2.2.1 Signal Seed; 2.2.2 Memory Latency; 2.3 Power Consumption and Noise; 2.3.1 Noise 2.4 Form Factor2.4.1 Non-Volatile Memory Technology: Flash; 2.4.2 Volatile Memory Technology: SRAM and DRAM; 2.4.3 CMOS Image Sensors; 2.5 Lower Cost; 2.6 Application Based Drivers; 2.6.1 Microprocessors; 2.6.2 Memory; 2.6.3 Sensors; 2.6.4 Fields Programmable Gate Arrays (FPGAs); References; 3 Overview of 3D

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7.1 Parylene

Sommario/riassunto

The first encompassing treatise of this new, but very important field puts the known physical limitations for classic 2D electronics into perspective with the requirements for further electronics developments and market necessities. This two-volume handbook presents 3D solutions to the feature density problem, addressing all important issues, such as wafer processing, die bonding, packaging technology, and thermal aspects.It begins with an introductory part, which defines necessary goals, existing issues and relates 3D integration to the semiconductor roadmap of the industry. Before going