1.	Record Nr.	UNINA9910791313803321
	Autore	Pollak Susan M.
	Titolo	Sitting together : essential skills for mindfulness-based psychotherapy / / Susan M. Pollak, Thomas Pedulla, and Ronald D. Siegel
	Pubbl/distr/stampa	New York : , : Guilford Press, , [2014] ©2014
	ISBN	1-4619-5839-3 1-4625-1399-9
	Descrizione fisica	1 online resource (258 p.)
	Disciplina	232 232.1
	Soggetti	Mindfulness-based cognitive therapy Meditation - Therapeutic use Psychotherapy
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Description based upon print version of record.
	Nota di bibliografia	Includes bibliographical references and index.
	Nota di contenuto	Bringing mindfulness into psychotherapy -- Becoming a mindful therapist -- Cultivating mindfulness in the therapeutic relationship -- Concentration practice : focusing the mind -- Open monitoring : expanding the mind -- Loving-kindness and compassion practice: engaging the heart -- Equanimity practice : finding balance -- Making mindfulness accessible -- The art of sequencing -- Beyond symptom relief : deepening mindfulness.
	Sommario/riassunto	This practical guide helps therapists from virtually any specialty or theoretical orientation choose and adapt mindfulness practices most likely to be effective with particular patients, while avoiding those that are contraindicated. The authors provide a wide range of meditations that build the core skills of focused attention, mindfulness, and compassionate acceptance. Vivid clinical examples show how to weave the practices into therapy, tailor them to each patient's needs, and overcome obstacles. Therapists also learn how developing their own mindfulness practice can enhance the

2.	Record Nr.	UNINA9910827660703321
	Autore	Prince Betty
	Titolo	Vertical 3D memory technologies / / Betty Prince
	Pubbl/distr/stampa	Chichester, England : , : Wiley, , 2014 ©2014
	ISBN	1-118-76046-8 1-118-76047-6 1-118-76045-X
	Edizione	[1st edition]
	Descrizione fisica	1 online resource (371 p.)
	Disciplina	621.39/732
	Soggetti	Three-dimensional integrated circuits Semiconductor storage devices
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Description based upon print version of record.
	Nota di bibliografia	Includes bibliographical references and index.
	Nota di contenuto	Vertical 3D Memory Technologies; Contents; Acknowledgments; 1 Basic Memory Device Trends Toward the Vertical; 1.1 Overview of 3D Vertical Memory Book; 1.2 Moore's Law and Scaling; 1.3 Early RAM 3D Memory; 1.3.1 SRAM as the First 3D Memory; 1.3.2 An Early 3D Memory-The FinFET SRAM; 1.3.3 Early Progress in 3D DRAM Trench and Stack Capacitors; 1.3.4 3D as the Next Step for Embedded RAM; 1.4 Early Nonvolatile Memories Evolve to 3D; 1.4.1 NOR Flash Memory-Both Standalone and Embedded; 1.4.2 The Charge-Trapping EEPROM; 1.4.3 Thin-Film Transistor Takes Nonvolatile Memory into 3D 1.4.4 3D Microcontroller Stacks with Embedded SRAM and EEPROM1. 4.5 NAND Flash Memory as an Ideal 3D Memory; 1.5 3D Cross-Point Arrays with Resistance RAM; 1.6 STT-MTJ Resistance Switches in 3D; 1.7 The Role of Emerging Memories in 3D Vertical Memories; References; 2 3D Memory Using Double-Gate, Folded, TFT, and Stacked Crystal Silicon; 2.1 Introduction; 2.2 FinFET-Early Vertical Memories; 2.2.1 Early FD-SOI FinFET Charge-Trapping Flash Memory; 2.2.2 FinFET Charge-Trapping Memory on Bulk Silicon; 2.2.3 Doubling Memory Density Using a Paired FinFET Bit-Line Structure 2.2.4 Other Folded Gate Memory Structures and Characteristics2.3 Double-Gate and Tri-Gate Flash; 2.3.1 Vertical Channel Double Floating

Sommario/riassunto	The large scale integration and planar scaling of individual system chips is reaching an expensive limit. If individual chips now, and later terrabyte memory blocks, memory macros, and processing cores, can be tightly linked in optimally designed and processed small footprint vertical stacks, then performance can be increased, power reduced and cost contained. This book reviews for the electronics industry engineer, professional and student the critical areas of development for 3D vertical memory chips including: gate-all-around and junction-less nanowire memories, stacked thin film and doubl