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Autore	Prince Betty
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2.5.4 Eight-Layer 3D Vertical DG TFT NAND Flash with Junctionless Buried Channel2.5.5 Variability in Polysilicon TFT for 3D Vertical Gate NAND Flash; 2.6 Stacked Gated Twin-Bit (SGTB) CT Flash; 2.7 Crystalline Silicon and Epitaxial Stacked Layers; 2.7.1 Stacked Crystalline Silicon Layer TFT for Six-Transistor SRAM Cell Technology; 2.7.2 Stacked Silicon Layer S3 Process for Production SRAM; 2.7.3 NAND Flash Memory Development Using Double-Stacked S3 Technology; 2.7.4 4Gb NAND Flash Memory in 45 nm 3D Double-Stacked S3 Technology; References; 3 Gate-All-Around (GAA) Nanowire for Vertical Memory
3.1 Overview of GAA Nanowire Memories

Sommario/riassunto

The large scale integration and planar scaling of individual system chips is reaching an expensive limit. If individual chips now, and later terrabyte memory blocks, memory macros, and processing cores, can be tightly linked in optimally designed and processed small footprint vertical stacks, then performance can be increased, power reduced and cost contained. This book reviews for the electronics industry engineer, professional and student the critical areas of development for 3D vertical memory chips including: gate-all-around and junction-less nanowire memories, stacked thin film and doubl