1. Record Nr. UNISA990000421190203316

Autore	ARACRI, Antonia
Titolo	Federalismo fiscale e omogeneità di trattamento / Antonia Aracri
Pubbl/distr/stampa	Torino : G. Giappichelli, 1996
ISBN	88-348-6053-5
Descrizione fisica	IX, 261 p. ; 24 cm
Collana	Quaderni del dipartimento di diritto pubblico ; 4
Disciplina	343.45043
Soggetti	Federalismo fiscale
Collocazione	XXIV.1. Coll. 10/ 5 (X 19 XIII 4)
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9910826714103321

Autore	Flynn Michael J
Titolo	Computer System Design : System-on-Chip
Pubbl/distr/stampa	Hoboken, : Wiley, 2011
ISBN	9786613157355 9781283157353 1283157357 9781118009918 1118009916 9781118009925 1118009924 9781118009901 1118009908
Edizione	[1st edition]
Descrizione fisica	1 online resource (356 p.)
Altri autori (Persone)	LukWayne
Disciplina	004.1
Soggetti	Systems on a chip Electrical & Computer Engineering Engineering & Applied Sciences Electrical Engineering

Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references (p. 316-328) and index.
Nota di contenuto	COMPUTER SYSTEM DESIGN; CONTENTS; PREFACE; LIST OF ABBREVIATIONS AND ACRONYMS; 1: Introduction to the Systems Approach; 1.1 SYSTEM ARCHITECTURE: AN OVERVIEW; 1.2 COMPONENTS OF THE SYSTEM: PROCESSORS, MEMORIES, AND INTERCONNECTS; 1.3 HARDWARE AND SOFTWARE: PROGRAMMABILITY VERSUS PERFORMANCE; 1.4 PROCESSOR ARCHITECTURES; 1.4.1 Processor: A Functional View; 1.4.2 Processor: An Architectural View; 1.5 MEMORY AND ADDRESSING; 1.5.1 SOC Memory Examples; 1.5.2 Addressing: The Architecture of Memory; 1.5.3 Memory for SOC Operating System; 1.6 SYSTEM-LEVEL INTERCONNECTION; 1.6.1 Bus-Based Approach 1.6.2 Network-on-Chip Approach1.7 AN APPROACH FOR SOC DESIGN; 1.7.1 Requirements and Specifications; 1.7.2 Design Iteration; 1.8 SYSTEM ARCHITECTURE AND COMPLEXITY; 1.9 PRODUCT ECONOMICS AND IMPLICATIONS FOR SOC; 1.9.1 Factors Affecting Product Costs; 1.9.2 Modeling Product Economics and Technology Complexity: The Lesson for SOC; 1.10 DEALING WITH DESIGN COMPLEXITY; 1.10.1 Buying IP; 1.10.2 Reconfiguration; 1.11 CONCLUSIONS; 1.12 PROBLEM SET; 2: Chip Basics: Time, Area, Power, Reliability, and Configurability; 2.1 INTRODUCTION; 2.1.1 Design Trade-Offs; 2.1.2 Requirements and Specifications 2.2 CYCLE TIME2.2.1 Defining a Cycle; 2.2.2 Optimum Pipeline; 2.2.3 Performance; 2.3 DIE AREA AND COST; 2.3.1 Processor Area; 2.3.2 Processor Subunits; 2.4 IDEAL AND PRACTICAL SCALING; 2.5 POWER; 2.6 AREA-TIME-POWER TRADE-OFFS IN PROCESSOR DESIGN; 2.6.1 Workstation Processor; 2.6.2 Embedded Processor; 2.7 RELIABILITY; 2.7.1 Dealing with Physical Faults; 2.7.2 Error Detection and Correction; 2.7.3 Dealing with Manufacturing Faults; 2.7.4 Memory and Function Scrubbing; 2.8 CONFIGURABILITY; 2.8.1 Why Reconfigurable Design?; 2.8.2 Area Estimate of Reconfigurable Devices; 2.9 CONCLUSION 2.10 PROBLEM SET3: Processors; 3.1 INTRODUCTION; 3.2 PROCESSOR SELECTION FOR SOC; 3.2.1 Overview; 3.2.2 Example: Soft Processors; 3.2.3 Examples: Processor Core Selection; 3.3 BASIC CONCEPTS IN PROCESSOR ARCHITECTURE; 3.3.1 Instruction Set; 3.3.2 Some Instruction Set Conventions; 3.3.3 Branches; 3.3.4 Interrupts and Exceptions; 3.4 BASIC CONCEPTS IN PROCESSOR MICROARCHITECTURE; 3.5 BASIC ELEMENTS IN INSTRUCTION HANDLING; 3.5.1 The Instruction Decoder and Interlocks; 3.5.2 Bypassing; 3.5.3 Execution Unit; 3.6 BUFFERS: MINIMIZING PIPELINE DELAYS; 3.6.1 Mean Request Rate Buffers 3.6.2 Buffers Designed for a Fixed or Maximum Request Rate3.7 BRANCHES: REDUCING THE COST OF BRANCHES; 3.7.1 Branch Target Capture: Branch Target Buffers (BTBs); 3.7.2 Branch Prediction; 3.8 MORE ROBUST PROCESSORS: VECTOR, VERY LONG INSTRUCTION WORD (VLIW), AND SUPERSCALAR; 3.9 VECTOR PROCESSORS AND VECTOR INSTRUCTION EXTENSIONS; 3.9.1 Vector Functional Units; 3.10 VLIW PROCESSORS; 3.11 SUPERSCALAR PROCESSORS; 3.11.1 Data Dependencies; 3.11.2 Detecting Instruction Concurrency; 3.11.3 A Simple Implementation; 3.11.4 Preserving State with Out-of-Order Execution 3.12 PROCESSOR EVOLUTION AND TWO EXAMPLES

Sommario/riassunto

The next generation of computer system designers will be less concerned about details of processors and memories, and more concerned about the elements of a system tailored to particular applications. These designers will have a fundamental knowledge of processors and other elements in the system, but the success of their design will depend on the skills in making system-level tradeoffs that optimize the cost, performance and other attributes to meet application requirements. This book provides a new treatment of computer system design, particularly for System-on-Chip (SOC), which addresses th