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2.2 CYCLE TIME2.2.1 Defining a Cycle; 2.2.2 Optimum Pipeline; 2.2.3 Performance; 2.3 DIE AREA AND COST; 2.3.1 Processor Area; 2.3.2 Processor Subunits; 2.4 IDEAL AND PRACTICAL SCALING; 2.5 POWER; 2.6 AREA-TIME-POWER TRADE-OFFS IN PROCESSOR DESIGN; 2.6.1 Workstation Processor; 2.6.2 Embedded Processor; 2.7 RELIABILITY; 2.7.1 Dealing with Physical Faults; 2.7.2 Error Detection and Correction; 2.7.3 Dealing with Manufacturing Faults; 2.7.4 Memory and Function Scrubbing; 2.8 CONFIGURABILITY; 2.8.1 Why Reconfigurable Design?; 2.8.2 Area Estimate of Reconfigurable Devices; 2.9 CONCLUSION
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3.12 PROCESSOR EVOLUTION AND TWO EXAMPLES

Sommario/riassunto

The next generation of computer system designers will be less concerned about details of processors and memories, and more concerned about the elements of a system tailored to particular applications. These designers will have a fundamental knowledge of processors and other elements in the system, but the success of their design will depend on the skills in making system-level tradeoffs that optimize the cost, performance and other attributes to meet application requirements. This book provides a new treatment of computer system design, particularly for System-on-Chip (SOC), which addresses th