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Nota di contenuto	Advanced Interconnects for ULSI Technology; Contents; About the Editors; List of Contributors; Preface; Abbreviations; Section I Low-k Materials; 1 Low-k Materials: Recent Advances; 1.1 Introduction; 1.2 Integration Challenges; 1.2.1 Process-Induced Damage; 1.2.2 Mechanical Properties; 1.3 Processing Approaches to Existing Integration Issues; 1.3.1 Post-deposition Treatments; 1.3.2 Prevention or Repair of Plasma-Induced Processing Damage; 1.3.3 Multilayer Structures; 1.4 Material Advances to Overcome Current Limitations; 1.4.1 Silica Zeolites; 1.4.2 Hybrid Organic-Inorganic: Oxycarbosilanes 1.5 ConclusionReferences; 2 Ultra-Low-k by CVD: Deposition and Curing; 2.1 Introduction; 2.2 Porogen Approach by PECVD; 2.2.1

Precursors and Deposition Conditions; 2.2.2 Mystery Still Unsolved: From Porogens to Pores; 2.3 UV Curing; 2.3.1 General Overview of Curing; 2.3.2 UV Curing Mechanisms; 2.4 Impact of Curing on Structure and Physical Properties: Benefits of UV Curing; 2.4.1 Porosity; 2.4.2 Chemical Structure and Mechanical Properties; 2.4.3 Electrical Properties; 2.5 Limit/Issues with the Porogen Approach; 2.5.1 Porosity Creation Limit; 2.5.2 Porogen Residues; 2.6 Future of CVD Low-k 2.6.1 New Matrix Precursor2.6.2 Other Deposition Strategies; 2.6.3 New Deposition Techniques; 2.7 Material Engineering: Adaptation to Integration Schemes; 2.8 Conclusion; References; 3 Plasma Processing of Low-k Dielectrics; 3.1 Introduction; 3.2 Materials and Equipment; 3.3 Process Results Characterization; 3.4 Interaction of Low-k Dielectrics with Plasma; 3.4.1 Low-k Etch Chemistries; 3.4.2 Patterning Strategies and Masking Materials; 3.4.3 Etch Mechanisms; 3.5 Mechanisms of Plasma Damage; 3.5.1 Gap Structure Studies; 3.5.2 Effect of Radical Density; 3.5.3 Effect of Ion Energy 3.5.4 Effect of Photon Energy and Intensity3.5.5 Plasma Damage by Oxidative Radicals; 3.5.6 Hydrogen-Based Plasma; 3.5.7 Minimization of Plasma Damage; 3.6 Dielectric Recovery; 3.6.1 CH<sub>4</sub> Beam Treatment; 3.6.2 Dielectric Recovery by Silylation; 3.6.3 UV Radiation; 3.7 Conclusions; References; 4 Wet Clean Applications in Porous Low-k Patterning Processes; 4.1 Introduction; 4.2 Silica and Porous Hybrid Dielectric Materials; 4.3 Impact of Plasma and Subsequent Wet Clean Processes on the Stability of Porous Low-k Dielectrics; 4.3.1 Stability in Pure Chemical Solutions 4.3.2 Stability in Commercial Chemistries4.3.3 Hydrophobicity of Hybrid Low-k Materials; 4.4 Removal of Post-Etch Residues and Copper Surface Cleaning; 4.5 Plasma Modification and Removal of Post-Etch 193 nm Photoresist; 4.5.1 Modification of 193 nm Photoresist by Plasma Etch; 4.5.2 Wet Removal of 193 nm Photoresist; Acknowledgments; References; Section II Conductive Layers and Barriers; 5 Copper Electroplating for On-Chip Metallization; 5.1 Introduction; 5.2 Copper Electroplating Techniques; 5.3 Copper Electroplating Superfill; 5.3.1 The Role of Accelerator; 5.3.2 The Role of Suppressor 5.3.3 The Role of Leveler

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## Sommario/riassunto

Finding new materials for copper/low-k interconnects is critical to the continuing development of computer chips. While copper/low-k interconnects have served well, allowing for the creation of Ultra Large Scale Integration (ULSI) devices which combine over a billion transistors onto a single chip, the increased resistance and RC-delay at the smaller scale has become a significant factor affecting chip performance. Advanced Interconnects for ULSI Technology is dedicated to the materials and methods which might be suitable replacements. It covers a broad range of topics, from physical

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