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Nota di contenuto	Cover; Contents; Foreword; Acknowledgments; About the Authors; Chapter 1: IC Fabrication Overview; Section 1: Introduction; 1.1 Integrated Circuits; 1.2 The Semiconductor Industry; Section 2: Support Technologies; 2.1 Crystal Growth and Wafer Preparation; 2.2 Contamination Control; 2.3 Circuit Design and Mask Making; 2.4 Process Diagnostics and Metrology; Section 3: Integrated Circuit Fabrication; 3.1 Layering; 3.2 Patterning; 3.3 Doping; 3.4 Process Control and In-line Monitoring; Section 4: Test and Assembly; 4.1 Electrical Tests; 4.2 Die Separation; 4.3 Die Attach and Wire Bonding 4.4 Encapsulation4.5 Final Test; Section 5: Summary; Chapter 2: Support Technologies; Section 1: Introduction; Section 2: Contamination Control; 2.1 Why Control Contamination?; 2.2 Contamination Sources; 2.3 The Cleanroom; Section 3: Crystal Growth and Wafer Preparation; 3.1 Introduction; 3.2 Silicon Purification; 3.3 Czochralski Silicon Growth; 3.4 Shaping, Grinding, Cutting and Polishing; 3.5 Final Inspection and Shipping; Section 4: Circuit Design; 4.1 Introduction; 4.2 Product Definition and New Product Plan; 4.3 The Design Team; 4.4 The Design Process; 4.5 Design Verification and

Tapeout

Section 5: Photomask and Reticle Preparation 5.1 Introduction; 5.2 Reticle Substrate Preparation; 5.3 Pattern Transfer; 5.4 Inspection and Defect Repair; Chapter 3: Forming Wells; Section 1: Introduction; Section 2: Initial Oxidation; Section 3: Photolithography; 3.1 Introduction; 3.2 Coat (Spin); 3.3 Exposure (Step); 3.4 Develop; 3.5 After Develop Inspect (ADI); Section 4: Ion Implantation; Chapter 4: Isolate Active Areas (Shallow Trench Isolation); Section 1: Introduction to Shallow Trench Isolation; Section 2: Pad Oxide Growth; Section 3: Silicon Nitride Deposition
Section 4: Photolithography for Photo/Etch Section 5: Hard Mask Formation Using Plasma Etch; 5.1 Hard Mask Overview; 5.2 Plasma Etch Overview; 5.3 Etch Chemistry: Silicon Dioxide and Silicon Nitride; Section 6: Form Trenches in Silicon with Plasma Etch; Section 7: Fill Trenches with Silicon Dioxide; Section 8: Chemical Mechanical Polishing (CMP) to Remove Excess Dioxide; Section 9: Wet Etch Removal of Silicon Nitride and Pad Oxide; Chapter 5: Building the Transistors; Section 1: Introduction; Section 2: Thin Film Formation; 2.1 Gate Dielectric Oxidation
2.2 Polycrystalline Silicon (Poly) Deposition 2.3 Nitride Cap Deposition; Section 3: Poly Gate Formation; 3.1 Photoresist Patterning; 3.2 Plasma Etch; Section 4: Source/Drain Formation; 4.1 Introduction; 4.2 Shallow Implant; 4.3 Spacer Formation; 4.4 High-Dose Implant; 4.5 Anneal; Section 5: Salicide Formation; 5.1 Sputter Cobalt; 5.2 RTP Reaction Forming Silicide; 5.3 Strip Residual Cobalt; 5.4 Anneal the Silicide; Chapter 6: First Level Metallization; Section 1: Introduction; Section 2: Nitride and Oxide Depositions; 2.1 Nitride Deposition; 2.2 Oxide Deposition; Section 3: CMP Planarization
Section 4: Photo/Etch for Contact Holes

Sommario/riassunto

This book takes the reader through the actual manufacturing process of making a typical chip, from start to finish, including a detailed discussion of each step, in plain language. The evolution of today's technology is added to the story, as seen through the eyes of the engineers who solved some of the problems. The authors are well suited to that discussion since they are three of those same engineers. They have a broad exposure to the industry and its technology that extends all the way back to Shockley Laboratories, the first semiconductor manufacturer in Silicon Valley. The CMOS (C
