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Nota di contenuto	Intro -- Contents -- Notices -- Trademarks -- Preface -- The specialists who wrote this redbook -- Become a published author -- Comments welcome -- Part 1 Virtualization technology -- Chapter 1. Introduction -- 1.1 Performance tuning redefined -- 1.1.1 Understanding performance -- 1.1.2 Performance considerations -- Chapter 2. IBM POWER5 architecture -- 2.1 Introduction -- 2.2 Chip design -- 2.3 POWER5 enhancements -- 2.4 POWER5 instruction pipelines -- 2.4.1 Instruction fetching -- 2.4.2 Branch prediction -- 2.4.3 Instruction decoding and preprocessing -- 2.4.4 Group dispatch -- 2.4.5 Register renaming -- 2.4.6 Instruction execution -- 2.5 Caches -- 2.5.1 Level 2 (L2) cache -- 2.5.2 Level 3 (L3) cache -- 2.5.3 Summary of caches on POWER5 -- 2.5.4 Address translation resources -- 2.6 Timing facilities -- 2.7 Dynamic power management -- 2.8 Processor Utilization Resource Register (PURR) -- 2.9 Large POWER5 SMPs -- 2.10 Summary -- Chapter 3. Simultaneous multithreading -- 3.1 What is multithreading? -- 3.2 POWER5 simultaneous multithreading features -- 3.2.1 Dynamic switching of thread states -- 3.2.2 Snooze and snooze delay -- 3.3 Controlling priority of threads -- 3.3.1 Dynamic resource balancing (DRB) -- 3.3.2 Adjustable thread priorities -- 3.3.3 Thread priority implementation -- 3.4 Software considerations -- 3.4.1 Simultaneous multithreading aware scheduling -- 3.4.2 Thread priorities on AIX 5L V5.3 -- 3.4.3 Thread priorities on Linux -- 3.4.4 Cache effects -- 3.5 Simultaneous multithreading

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