

1. Record Nr.	UNINA9910823677003321
Titolo	Design of high-speed communication circuits // editor, Ramesh Harjani
Pubbl/distr/stampa	New Jersey, : World Scientific, 2006
ISBN	1-281-37920-4 9786611379209 981-277-458-0
Edizione	[1st ed.]
Descrizione fisica	1 online resource (232 p.)
Collana	Selected topics in electronics and systems ; ; v. 38
Altri autori (Persone)	HarjaniRamesh <1959->
Disciplina	621.3192
Soggetti	Electric circuits - Design and construction Electrical engineering
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references.
Nota di contenuto	CONTENTS; Preface; Achieving Analog Accuracy in Nanometer CMOS; 1 Introduction; 2 Transistor Mismatch; 3 Methods of Achieving Yield; 4 Alternative Techniques for Nanometer CMOS; References; Self-Induced Noise in Integrated Circuits; 1 Introduction 2 Self-Induced Noise-Injection and Sensing Mechanisms 3 Extraction of Substrate Parasitics; 4 Conclusions; References; High-Speed Oversampling Analog-to-Digital Converters; 1 Introduction; 2 Single-Loop AE Modulator Topologies; 3 Time-Interleaved AE Modulators 4 Continuous-Time AE Modulators 5 Conclusions; References; Designing LC VCOs Using Capacitive Degeneration Techniques; 1 Introduction; 2 LC Tank-based VCO Design; 3 Design Examples; 4 Summary and Conclusions; References Integrated Frequency Synthesizers: A Tutorial 1 Introduction 2 Interpreting Specifications; 3 Types of Frequency Synthesizers; 4 Phase Locked Loop (PLL) Design; 5 Recent Progress in Frequency Synthesizer Design Techniques; 6 Conclusion; References Recent Advances and Design Trends in CMOS Radio Frequency Integrated Circuits 1 Introduction; 2 Radio Receiver Architectures; 3 Low Noise Amplifiers; 4 Mixers; 5 Voltage-controlled Oscillators; References; Equalizers for High-Speed Serial Links ; 1 Introduction

2 Channel Modeling

Sommario/riassunto

MOS technology has rapidly become the de facto standard for mixed-signal integrated circuit design due to the high levels of integration possible as device geometries shrink to nanometer scales. The reduction in feature size means that the number of transistor and clock speeds have increased significantly. In fact, current day microprocessors contain hundreds of millions of transistors operating at multiple gigahertz. Furthermore, this reduction in feature size also has a significant impact on mixed-signal circuits. Due to the higher levels of integration, the majority of ASICs possess
