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Based Testability Analysis; Simulation-Based Testability Analysis; RTL Testability Analysis; Design for Testability Basics; Ad Hoc Approach; Test Point Insertion; Structured Approach; Scan Cell Designs; Muxed-D Scan Cell; Clocked-Scan Cell; LSSD Scan Cell; Scan Architectures; Full-Scan Design; Muxed-D Full-Scan Design; Clocked Full-Scan Design; LSSD Full-Scan Design; Partial-Scan Design; Random-Access Scan Design; Scan Design Rules; Tristate Buses; Bidirectional I/O Ports; Gated Clocks; Derived Clocks
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References 3 Logic and Fault Simulation; Introduction; Logic Simulation for Design Verification; Fault Simulation for Test and Diagnosis; Simulation Models; Gate-Level Network; Sequential Circuits; Logic Symbols; Unknown State u; High-Impedance State Z; Intermediate Logic States; Logic Element Evaluation; Truth Tables; Input Scanning; Input Counting; Parallel Gate Evaluation; Timing Models; Transport Delay; Inertial Delay; Wire Delay; Functional Element Delay Model; Logic Simulation; Compiled-Code Simulation; Logic Optimization; Logic Levelization; Code Generation; Event-Driven Simulation
Nominal-Delay Event-Driven Simulation

Sommario/riassunto

This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product, drive down test cost, improve product quality and yield, and speed up time-to-market and time-to-volume.· Most up-to-date coverage of design for testability. · Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. · Numerous, practical examples in each chapter illustrating basic VLSI test principles and DFT architectures.· Lecture slides and exercise solutions for all chapters are now available.·