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| Nota di contenuto | Front Cover; System-on-Chip Test Architectures; Copyright Page; Table of Contents; Preface; In the Classroom; Acknowledgments; Contributors; About the Editors; Chapter 1 Introduction; 1.1 Importance of System-on-Chip Testing; 1.1.1 Yield and Reject Rate; 1.1.2 Reliability and System Availability; 1.2 Basics of SOC Testing; 1.2.1 Boundary Scan (IEEE 1149.1 Standard); 1.2.2 Boundary Scan Extension (IEEE 1149.6 Standard); 1.2.3 Boundary-Scan Accessible Embedded Instruments (IEEE P1687); 1.2.4 Core-Based Testing (IEEE 1500 Standard); 1.2.5 Analog Boundary Scan (IEEE 1149.4 Standard) 1.3 Basics of Memory Testing1.4 SOC Design Examples; 1.4.1 BioMEMS Sensor; 1.4.2 Network-on-Chip Processor; 1.5 About This Book; 1.5.1 DFT Architectures; 1.5.2 New Fault Models and Advanced Techniques; 1.5.3 Yield and Reliability Enhancement; 1.5.4 Nanotechnology Testing Aspects; 1.6 Exercises; Acknowledgments; References; Chapter 2 Digital Test Architectures; 2.1 Introduction; 2.2 Scan Design; 2.2.1 Scan Architectures; 2.2.1.1 Muxed-D Scan Design; 2.2.1.2 Clocked-Scan Design; 2.2.1.3 LSSD Scan Design; 2.2.1.4 Enhanced-Scan Design; |

2.2.2 Low-Power Scan Architectures

2.2.2.1 Reduced-Voltage Low-Power Scan Design2.2.2.2 Reduced-Frequency Low-Power Scan Design; 2.2.2.3 Multi-Phase or Multi-Duty Low-Power Scan Design; 2.2.2.4 Bandwidth-Matching Low-Power Scan Design; 2.2.2.5 Hybrid Low-Power Scan Design; 2.2.3 At-Speed Scan Architectures; 2.3 Logic Built-In Self-Test; 2.3.1 Logic BIST Architectures; 2.3.1.1 Self-Testing Using MISR and Parallel SRSG (STUMPS); 2.3.1.2 Concurrent Built-In Logic Block Observer (CBILBO); 2.3.2 Coverage-Driven Logic BIST Architectures; 2.3.2.1 Weighted Pattern Generation; 2.3.2.2 Test Point Insertion; 2.3.2.3 Mixed-Mode BIST

2.3.2.4 Hybrid BIST2.3.3 Low-Power Logic BIST Architectures; 2.3.3.1 Low-Transition BIST Design; 2.3.3.2 Test-Vector-Inhibiting BIST Design; 2.3.3.3 Modified LFSR Low-Power BIST Design; 2.3.4 At-Speed Logic BIST Architectures; 2.3.4.1 Single-Capture; 2.3.4.2 Skewed-Load; 2.3.4.3 Double-Capture; 2.3.5 Industry Practices; 2.4 Test Compression; 2.4.1 Circuits for Test Stimulus Compression; 2.4.1.1 Linear-Decompression-Based Schemes; 2.4.1.2 Broadcast-Scan-Based Schemes; 2.4.1.3 Comparison; 2.4.2 Circuits for Test Response Compaction; 2.4.2.1 Space Compaction; 2.4.2.2 Time Compaction

2.4.2.3 Mixed Time and Space Compaction2.4.3 Low-Power Test Compression Architectures; 2.4.4 Industry Practices; 2.5 Random-Access Scan Design; 2.5.1 Random-Access Scan Architectures; 2.5.1.1 Progressive Random-Access Scan Design; 2.5.1.2 Shift-Addressable Random-Access Scan Design; 2.5.2 Test Compression RAS Architectures; 2.5.3 At-Speed RAS Architectures; 2.6 Concluding Remarks; 2.7 Exercises; Acknowledgments; References; Chapter 3 Fault-Tolerant Design; 3.1 Introduction; 3.2 Fundamentals of Fault Tolerance; 3.2.1 Reliability; 3.2.2 Mean Time to Failure (MTTF); 3.2.3 Maintainability

3.2.4 Availability

Sommario/riassunto

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers.  As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost.  This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master qu