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Autore	Minns Peter D
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Nota di contenuto	FSM-based Digital Design using Verilog HDL; Contents; Preface; Acknowledgements; 1 Introduction to Finite-State Machines and State Diagrams for the Design of Electronic Circuits and Systems; 1.1 INTRODUCTION; 1.2 LEARNING MATERIAL; 1.3 SUMMARY; 2 Using State Diagrams to Control External Hardware Subsystems; 2.1 INTRODUCTION; 2.2 LEARNING MATERIAL; 2.3 SUMMARY; 3 Synthesizing Hardware from a State Diagram; 3.1 INTRODUCTION TO FINITE-STATE MACHINE SYNTHESIS; 3.2 LEARNING MATERIAL; 3.3 SUMMARY; 4 Synchronous Finite-State Machine Designs; 4.1 TRADITIONAL STATE DIAGRAM SYNTHESIS METHOD 4.2 DEALING WITH UNUSED STATES4.3 DEVELOPMENT OF A HIGH/LOW ALARM INDICATOR SYSTEM; 4.3.1 Testing the Finite-State Machine using a Test-Bench Module; 4.4 SIMPLE WAVEFORM GENERATOR; 4.4.1 Sampling Frequency and Samples per Waveform; 4.5 THE DICE GAME; 4.5.1 Development of the Equations for the Dice Game; 4.6 BINARY DATA SERIAL TRANSMITTER; 4.6.1 The RE Counter Block in the Shift

Register of Figure 4.15; 4.7 DEVELOPMENT OF A SERIAL ASYNCHRONOUS RECEIVER; 4.7.1 Finite-State Machine Equations; 4.8 ADDING PARITY DETECTION TO THE SERIAL RECEIVER SYSTEM; 4.8.1 To Incorporate the Parity  
 4.8.2 D-Type Equations for Figure 4.264.9 AN ASYNCHRONOUS SERIAL TRANSMITTER SYSTEM; 4.9.1 Equations for the Asynchronous Serial Transmitter; 4.10 CLOCKED WATCHDOG TIMER; 4.10.1 D Flip-Flop Equations; 4.10.2 Output Equation; 4.11 SUMMARY; 5 The One Hot Technique in Finite-State Machine Design; 5.1 THE ONE HOT TECHNIQUE; 5.2 A DATA ACQUISITION SYSTEM; 5.3 A SHARED MEMORY SYSTEM; 5.4 FAST WAVEFORM SYNTHESIZER; 5.4.1 Specification; 5.4.2 A Possible Solution; 5.4.3 Equations for the d Inputs to D Flip-Flops; 5.4.4 Output Equations  
 5.5 CONTROLLING THE FINITE-STATE MACHINE FROM A MICROPROCESSOR/MICROCONTROLLER5.6 A MEMORY-CHIP TESTER; 5.7 COMPARING ONE HOT WITH THE MORE CONVENTIONAL DESIGN METHOD OF CHAPTER 4; 5.8 A DYNAMIC MEMORY ACCESS CONTROLLER; 5.8.1 Flip-Flop Equations; 5.8.2 Output Equations; 5.9 HOW TO CONTROL THE DYNAMIC MEMORY ACCESS FROM A MICROPROCESSOR; 5.10 DETECTING SEQUENTIAL BINARY SEQUENCES USING A FINITE-STATE MACHINE; 5.11 SUMMARY; 6 Introduction to Verilog HDL; 6.1 A BRIEF BACKGROUND TO HARDWARE DESCRIPTION LANGUAGES; 6.2 HARDWARE MODELLING WITH VERILOG HDL: THE MODULE  
 6.3 MODULES WITHIN MODULES: CREATING HIERARCHY6.4 VERILOG HDL SIMULATION: A COMPLETE EXAMPLE; REFERENCES; 7 Elements of Verilog HDL; 7.1 BUILT-IN PRIMITIVES AND TYPES; 7.1.1 Verilog Types; 7.1.2 Verilog Logic and Numeric Values; 7.1.3 Specifying Values; 7.1.4 Verilog HDL Primitive Gates; 7.2 OPERATORS AND EXPRESSIONS; 7.3 EXAMPLE ILLUSTRATING THE USE OF VERILOG HDL OPERATORS: HAMMING CODE ENCODER; 7.3.1 Simulating the Hamming Encoder; REFERENCES; 8 Describing Combinational and Sequential Logic using Verilog HDL; 8.1 THE DATA-FLOW STYLE OF DESCRIPTION: REVIEW OF THE CONTINUOUS ASSIGNMENT  
 8.2 THE BEHAVIOURAL STYLE OF DESCRIPTION: THE SEQUENTIAL BLOCK

## Sommario/riassunto

As digital circuit elements decrease in physical size, resulting in increasingly complex systems, a basic logic model that can be used in the control and design of a range of semiconductor devices is vital. Finite State Machines (FSM) have numerous advantages; they can be applied to many areas (including motor control, and signal and serial data identification to name a few) and they use less logic than their alternatives, leading to the development of faster digital hardware systems. This clear and logical book presents a range of novel techniques for the rapid and reliable design of digit