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Nota di contenuto	ESD Failure Mechanisms and Models; Contents; About the Author; Preface; Acknowledgments; 1 Failure Analysis and ESD; 1.1 INTRODUCTION; 1.1.1 FA Techniques for Evaluation of ESD Events; 1.1.2 Fundamental Concepts of ESD FA Methods and Practices; 1.1.3 ESD Failure: Why Do Semiconductor Chips Fail?; 1.1.4 How to Use FA to Design ESD Robust Technologies; 1.1.5 How to Use FA to Design ESD Robust Circuits; 1.1.6 How to Use FA for Temperature Prediction; 1.1.7 How to Use Failure Models for Power Prediction; 1.1.8 FA Methods, Design Rules, and ESD Ground Rules 1.1.9 FA and Semiconductor Process-Induced ESD Design Asymmetry 1.1.10 FA Methodology and Electro-thermal Simulation; 1.1.11 FA and ESD Testing Methodology; 1.1.12 FA Methodology for Evaluation of ESD

Parasitics; 1.1.13 FA Methods and ESD Device Operation Verification; 1.1.14 FA Methodology to Evaluate Inter-power Rail Electrical Connectivity; 1.1.15 How to Use FA to Eliminate Failure Mechanisms; 1.2 ESD FAILURE: HOW DO MICRO-ELECTRONIC DEVICES FAIL?; 1.2.1 ESD Failure: How Do Metallurgical Junctions Fail?; 1.2.2 ESD Failure: How Do Insulators Fail?; 1.2.3 ESD Failure: How Do Metals Fail? 1.3 SENSITIVITY OF SEMICONDUCTOR COMPONENTS 1.3.1 ESD Sensitivity as a Function of Materials; 1.3.2 ESD Sensitivity as a Function of Semiconductor Devices; 1.3.3 ESD Sensitivity as a Function of Product Type; 1.3.4 ESD and Technology Scaling; 1.3.5 ESD Technology Roadmap; 1.4 HOW DO SEMICONDUCTOR CHIPS FAIL--ARE THE FAILURES RANDOM OR SYSTEMATIC?; 1.5 CLOSING COMMENTS AND SUMMARY; PROBLEMS; REFERENCES; 2 Failure Analysis Tools, Models, and Physics of Failure; 2.1 FA TECHNIQUES FOR EVALUATION OF ESD EVENTS; 2.2 FA TOOLS; 2.2.1 Optical Microscope; 2.2.2 Scanning Electron Microscope 2.2.3 Transmission Electron Microscope 2.2.4 Emission Microscope; 2.2.5 Thermally Induced Voltage Alteration; 2.2.6 Superconducting Quantum Interference Device Microscope; 2.2.7 Atomic Force Microscope; 2.2.8 The 2-D AFM; 2.2.9 Picosecond Current Analysis Tool; 2.2.10 Transmission Line Pulse--Pico second Current Analysis Tool; 2.3 ESD SIMULATION: ESD PULSE MODELS; 2.3.1 Human Body Model; 2.3.2 Machine Model; 2.3.3 Cassette Model; 2.3.4 Socketed Device Model; 2.3.5 Charged Board Model; 2.3.6 Cable Discharge Event; 2.3.7 IEC System-Level Pulse Model; 2.3.8 Human Metal Model 2.3.9 Transmission Line Pulse Testing 2.3.10 Very Fast Transmission Line Pulse (VF-TLP) Model; 2.3.11 Ultra-fast Transmission Line Pulse (UF-TLP) Model; 2.4 ELECTRO-THERMAL PHYSICAL MODELS; 2.4.1 Tasca Model; 2.4.2 Wunsch-Bell Model; 2.4.3 Smith-Littau Model; 2.4.4 Ash Model; 2.4.5 Arkhipov, Astvatsaturyan, Godovosyn, and Rudenko Model; 2.4.6 Dwyer, Franklin, and Campbell Model; 2.4.7 Vlasov-Sinkevitch Model; 2.5 STATISTICAL MODELS FOR ESD PREDICTION; 2.6 CLOSING COMMENTS AND SUMMARY; PROBLEMS; REFERENCES; 3 CMOS Failure Mechanisms; 3.1 TABLES OF CMOS ESD FAILURE MECHANISMS 3.2 LOCOS ISOLATION-DEFINED CMOS

Sommario/riassunto

Electrostatic discharge (ESD) failure mechanisms continue to impact semiconductor components and systems as technologies scale from micro- to nano-electronics. This book studies electrical overstress, ESD, and latchup from a failure analysis and case-study approach. It provides a clear insight into the physics of failure from a generalist perspective, followed by investigation of failure mechanisms in specific technologies, circuits, and systems. The book is unique in covering both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit method
