

1. Record Nr.	UNINA9910815642003321
Autore	Voldman Steven H.
Titolo	The ESD handbook // Steven H. Voldman
Pubbl/distr/stampa	Hoboken, New Jersey ; ; West Sussex, England : , : Wiley, , [2021] ©2021
ISBN	1-119-23310-0
Descrizione fisica	1 online resource (1,574 pages) : illustrations
Disciplina	537.52
Soggetti	Electric discharges
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	<p>Intro -- Table of Contents -- Title Page -- Copyright -- Dedication --</p> <p>About the Author -- Acknowledgements -- 1 ESD, EOS, EMI, EMC, and Latchup -- 1.1 Electrostatic Discharge (ESD) -- 1.2 Human Body Model (HBM) -- 1.3 Machine Model (MM) -- 1.4 Cassette Model -- 1.5 Charged Device Model (CDM) -- 1.6 Transmission Line Pulse (TLP) -- 1.7 Very Fast Transmission Line Pulse (VF-TLP) -- 1.8 Electrical Overstress (EOS) -- 1.9 Electrical Overstress (EOS) -- 1.10 EOS Sources - Lightning -- 1.11 EOS Sources - Electromagnetic Pulse (EMP) -- 1.12 EOS Sources - Machinery -- 1.13 EOS Sources - Power Distribution -- 1.14 EOS Sources - Switches, Relays, and Coils -- 1.15 EOS Design Flow and Product Definition -- 1.16 EOS Sources - Design Issues -- 1.17 Electromagnetic Interference (EMI) -- 1.18 Electromagnetic Compatibility (EMC) -- 1.19 Latchup -- Questions and Answers -- 1.20 Summary and Closing Comments -- References -- 2 ESD in Manufacturing -- 2.1 Flooring -- 2.2 Work Surfaces -- 2.3 Garments -- 2.4 Wrist Straps -- 2.5 Shoes - Footwear -- 2.6 Ionization -- 2.7 Clean Rooms -- 2.8 Carts -- 2.9 Shipping Tubes -- 2.10 Trays -- 2.11 Measurements -- 2.12 Verification -- 2.13 Audit -- 2.14 Triboelectric Charging - How Does it Happen? -- 2.15 Conductors, Semiconductors, and Insulators -- 2.16 Static Dissipative Materials -- 2.17 ESD and Materials -- 2.18 Electrification and Coulomb's Law -- 2.19 Electromagnetism and Electrodynamics -- 2.20 Electrical Breakdown -- 2.21 Electro-Quasistatics and Magnetoquasistatics -- 2.22 Electrodynamics and Maxwell's Equations -- 2.23 Electrostatic</p>

Discharge (ESD) -- 2.24 Electromagnetic Compatibility (EMC) -- 2.25
Electromagnetic Interference (EMI) -- 2.26 Fundamentals of
Manufacturing and Electrostatics -- 2.27 Materials, Tooling, Human
Factors, and Electrostatic Discharge -- 2.28 Materials and Human-
induced Electric Fields.
2.29 Manufacturing Environment and Tooling -- 2.30 Manufacturing
Equipment and ESD Manufacturing Problems -- 2.31 Manufacturing
Materials -- 2.32 Measurement and Test Equipment -- 2.33
Manufacturing Testing for Compliance -- 2.34 Grounding and Bonding
Systems -- 2.35 Work Surfaces -- 2.36 Wrist Straps -- 2.37 Constant
Monitors -- 2.38 Footwear -- 2.39 Floors -- 2.40 Personnel Grounding
with Garments -- 2.41 Garments -- 2.42 Air Ionization -- 2.43 Seating
-- 2.44 Packaging and Shipping -- 2.45 Trays -- 2.46 ESD
Identification -- 2.47 ESD Program Auditing -- 2.48 ESD On-Chip
Protection -- 2.49 ESD, EOS, EMI, EMC, and Latchup -- 2.50
Manufacturing Electrical Overstress (EOS) -- 2.51 EMI -- 2.52 EMC --
2.53 Summary and Closing Comments -- References -- 3 ESD
Standards -- 3.1 Factory - Flooring -- 3.2 Factory - Resistance
Measurement of Materials -- 3.3 JEDEC -- 3.4 International Electro-
Technical Commission (IEC) -- 3.5 IEEE -- 3.6 Department of Defense
(DOD) -- 3.7 Military Standards -- 3.8 SAE -- 3.9 Summary and
Closing Comments -- Questions and Answers -- References -- 4 ESD
Testing -- 4.1 Electrostatic Discharge (ESD) Testing -- 4.2 ESD Models
-- 4.3 HBM Test System -- 4.4 HBM Two-pin Test System -- 4.5
Machine Model (MM) -- 4.6 Small Charge Model (SCM) -- 4.7 Small
Charge Model Source -- 4.8 CDM Pulse Waveform -- 4.9 HMM
Equivalent Circuit -- 4.10 HMM Test Equipment -- 4.11 HMM Test
Configuration -- 4.12 HMM Fixture Board -- 4.13 Transmission Line
Pulse (TLP) -- 4.14 TLP Test Systems -- 4.15 IEC 61000-4-2 -- 4.16
Equivalent Circuit -- 4.17 Test Equipment -- 4.18 Cable Discharge
Event (CDE) -- 4.19 CDE Pulse Waveform -- 4.20 Equivalent Circuit --
4.21 Commercial Test Systems -- 4.22 Systems Electromagnetic
Interference (EMI) -- 4.23 Electromagnetic Compatibility (EMC) -- 4.24
Electrical Overstress (EOS) -- 4.25 Latchup.
4.26 Electrical Overstress (EOS) -- 4.27 EOS Sources - Lightning --
4.28 EOS Sources - Electromagnetic Pulse (EMP) -- 4.29
Electromagnetic Compatibility -- 4.30 Summary and Closing
Comments -- References -- 5 ESD Device Physics -- 5.1 Electro-
thermal Instability -- 5.2 Stable System -- 5.3 Unstable System -- 5.4
Differential Relation of Voltage and Current -- 5.5 Time Constant
Hierarchy -- 5.6 Thermal Physics Time Constants -- 5.7 Adiabatic,
Thermal Diffusion Time Scale and Steady State -- 5.8 Electro-
quasistatic and Magnetoquasistatics -- 5.9 Electrical Instability -- 5.10
Thermal Physics Time Constants -- 5.11 Adiabatic, Thermal Diffusion
Time Scale and Steady State -- 5.12 Electrical Instability and Breakdown
-- 5.13 Spatial Instability and Electro-thermal Current Constriction --
5.14 Equipotential Surface -- 5.15 Heat Flow -- 5.16 Conservation of
Heat -- 5.17 Electric Potential and Temperature Gradient -- 5.18
Electric Energy, Resistivity, and Thermal Conductivity -- 5.19
Breakdown -- 5.20 Electron Current Continuity Relationship -- 5.21 Air
Breakdown and Peak Currents -- 5.22 Electro-thermal Instability --
5.23 Mathematical Methods - Green's Function and Method of Images
-- 5.24 Mathematical Methods - Green's Function and Method of
Images -- 5.25 Mathematical Methods - Integral Transforms of the
Heat Conduction Equation -- 5.26 Flux Potential Transfer Relations
Matrix Methodology -- 5.27 Heat Equation Variable Conductivity --
5.28 Mathematical Methods - Boltzmann Transformation -- 5.29
Mathematical Methods - The Duhamel Formulation -- 5.30 Spherical

Source Tasca Model -- 5.31 Wunsch-Bell Model -- 5.32 The Smith and Littau Model -- 5.33 The Arkhipov-Astvatsaturyan-Godovosyn-Rudenko Model -- 5.34 The Vlasov-Sinkevitch Model -- 5.35 The Dwyer, Franklin and Campbell Model -- 5.36 Negative Differential Resistor and Resistor Ballasting.

5.37 Ash Model - Nonlinear Failure Power Thresholds -- 5.38 Statistical Models for ESD Prediction -- 5.39 Summary and Closing Comments -- References -- 6 ESD Events and Protection Circuits -- 6.1 Human Body Model (HBM) -- 6.2 Machine Model (MM) -- 6.3 Charged Device Model -- 6.4 Human Metal Model (HMM) -- 6.5 IEC 61000-4-2 History -- 6.6 IEC 61000-4-5 -- 6.7 Cable Discharge Event (CDE) -- 6.8 CDM Scope -- References -- 7 ESD Failure Mechanism -- 7.1 Tables of CMOS ESD Failure Mechanisms -- 7.2 LOCOS Isolation-Defined CMOS -- 7.3 LOCOS-bound Thick Oxide MOSFET -- 7.4 LOCOS-Bound Structures -- 7.5 Shallow Trench Isolation (STI) -- 7.6 STI Pull-down ESD Failure Mechanism -- 7.7 STI Pull-Down and Gate Wrap-Around -- 7.8 MOSFETs -- 7.9 LOCOS-bound Thick Oxide MOSFET -- 7.10 Bipolar Transistor Devices -- 7.11 Silicide Blocked N-diffusion Resistors -- 7.12 Silicon Germanium ESD Failure Mechanisms -- 7.13 Silicon Germanium Carbon ESD Failure Mechanisms -- 7.14 Gallium Arsenide Technology ESD Failure Mechanisms -- 7.15 Indium Gallium Arsenide ESD Failure Mechanisms -- 7.16 Micro Electromechanical (MEM) Systems -- 7.17 Micro-mirror Array Failures -- 7.18 EOS Bond Pad and Interconnect Failure -- 7.19 Summary and Closing Comments -- References -- 8 ESD Design Synthesis -- 8.1 ESD Design Synthesis and Architecture Flow -- 8.2 ESD Design - the Signal Path and the Alternate Current Path -- 8.3 ESD Electrical Circuit and Schematic Architecture Concepts -- 8.4 The Ideal ESD Network -- 8.5 Mapping Semiconductor Chips and ESD Designs -- 8.6 Mapping across Semiconductor Fabricators -- 8.7 ESD Design Mapping across Technology Generations -- 8.8 ESD Networks, Sequencing, and Chip Architecture -- 8.9 ESD Layout and Floorplan-related Concepts -- 8.10 ESD Architecture and Floor-planning -- 8.11 Digital and Analog CMOS Architecture.

8.12 Digital and Analog Floorplan - Placement of Analog Circuits -- 8.13 Mixed-signal Architecture - Digital, Analog, and RF Architecture -- 8.14 Summary and Closing Comments -- Questions -- References -- 9 On-chip ESD Protection Circuits - Input Circuitry -- 9.1 Receivers and ESD -- 9.2 Receivers and Receiver Delay Time -- 9.3 ESD Loading Effect on Receiver Performance -- 9.4 Receivers and HBM -- 9.5 Receivers and CDM -- 9.6 Receivers and Receiver Evolution -- 9.7 Receiver Circuits with Half-pass Transmission Gate -- 9.8 Receiver with Full-pass Transmission Gate -- 9.9 Receiver, Half-pass Transmission Gate, and Keeper Network -- 9.10 Receiver, Half-pass Transmission Gate, and the Modified Keeper Network -- 9.11 Receiver Circuits with Pseudo-zero VT Half-pass Transmission Gates -- 9.12 Receiver with Zero VT Transmission Gate -- 9.13 Receiver Circuits with Bleed Transistors -- 9.14 Receiver Circuits with Test Functions -- 9.15 Receiver with Schmitt Trigger Feedback Network -- 9.16 Bipolar Transistor Receivers -- 9.17 CMOS Differential Receiver with Analog Layout Concepts -- 9.18 CMOS Differential Receiver Capacitance Loading -- 9.19 CMOS Differential Receiver ESD Mismatch -- 9.20 Analog Differential Pair ESD Signal Pin Matching with Common Well Layout -- 9.21 Analog Differential Pair Common Centroid Design Layout - Signal-Pin to Signal-Pin and Parasitic ESD Elements -- 9.22 Off-chip Drivers (OCD) -- 9.23 Off-chip Driver I/O Standards and ESD -- 9.24 Off-chip Driver (OCD) ESD Design Basics -- 9.25 Off-chip Drivers (OCD): Mixed Voltage Interface -- 9.26 Off-chip Drivers (OCD): Self-bias Well OCD Networks -- 9.27 Self-bias Well Off-chip Driver

(OCD) Networks -- 9.28 ESD Protection Networks for Self-bias Well
OCD Networks -- 9.29 Programmable Impedance Off-chip Driver (OCD)
Network.

9.30 ESD Input Protection Networks for Programmable Impedance Off-chip Drivers.
