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3.3.1. Time-predictability issues raised by multithreading3.3.2. Time-predictable example architectures; 3.4. Branch prediction; 3.4.1. State-of-the-art branch prediction; 3.4.2. Branch prediction in real-time systems; 3.4.3. Approaches to branch prediction modeling; CHAPTER 4. MEMORY HIERARCHY; 4.1. Caches; 4.1.1. Organization of cache memories; 4.1.2. Static analysis of the behavior of caches; 4.1.3. Recommendations for timing predictability; 4.2. Scratchpad memories; 4.2.1. Scratchpad RAM; 4.2.2. Data scratchpad; 4.2.3. Instruction scratchpad; 4.3. External memories; 4.3.1. Static RAM
4.3.2. Dynamic RAM4.3.3. Flash memory; CHAPTER 5. MULTICORES; 5.1. Impact of resource sharing on time predictability; 5.2. Timing analysis for multicores; 5.2.1. Analysis of temporal/bandwidth sharing; 5.2.2. Analysis of spatial sharing; 5.3. Local caches; 5.3.1. Coherence techniques; 5.3.2. Discussion on timing analyzability; 5.4. Conclusion; 5.5. Time-predictable architectures; 5.5.1. Uncached accesses to shared data; 5.5.2. On-demand coherent cache; CHAPTER 6. EXAMPLE ARCHITECTURES; 6.1. The multithreaded processor Komodo; 6.1.1. The Komodo architecture; 6.1.2. Integrated thread scheduling
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6.5.4. Memory hierarchy

Sommario/riassunto

Building computers that can be used to design embedded real-time systems is the subject of this title. Real-time embedded software requires increasingly higher performances. The authors therefore consider processors that implement advanced mechanisms such as pipelining, out-of-order execution, branch prediction, cache memories, multi-threading, multicorearchitectures, etc. The authors of this book investigate the timepredictability of such schemes.