1. Record Nr. UNINA9910808850803321

Autore	Doman David
Titolo	Engineering the CMOS library : enhancing digital design kits for competitive silicon / / David Doman
Pubbl/distr/stampa	Hoboken, N.J., : John Wiley & Sons, c2012
ISBN	9786613621894 9781280592065 1280592060 9781118273135 1118273133 9781118273142 1118273141 9781118273111 1118273117
Edizione	[1st edition]
Descrizione fisica	1 online resource (343 p.)
Classificazione	TEC008050
Disciplina	621.3815
Soggetti	Digital integrated circuits - Design and construction Metal oxide semiconductors, Complementary Industrial efficiency
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di contenuto	Engineering the CMOS Library: Enhancing Digital Design Kits for Competitive Silicon; Contents; Preface; Acknowledgments; 1: Introduction; 1.1: Adding Project-Specific Functions, Drive Strengths, Views, and Corners; 1.2: What Is a DDK?; 2: Stdcell Libraries; 2.1: Lesson from the Real World: Manager's Perspective and Engineer's Perspective; 2.2: What Is a Stdcell?; 2.2.1: Combinational Functions; 2.2.2: Sequential Functions; 2.2.3: Clock Functions; 2.3: Extended Library Offerings; 2.3.1: Low-Power Support; 2.4: Boutique Library Offerings; 2.5: Concepts for Further Study; 3: IO Libraries 3.1: Lesson from the Real World: The Manager's Perspective and the Engineer's Perspective 3.2: Extension Capable Architectures versus Function Complete Architectures; 3.3: Electrostatic Discharge

Considerations; 3.3.1: Footprints; 3.3.2: Custom Design Versus Standard IO Design Comparison; 3.3.3: The Need for Maintaining Multiple IO Footprint Regions on an IC; 3.3.4: Circuit Under Pad; 3.4: Concepts for Further Study; 4: Memory Compilers; 4.1: Lesson from the Real World: The Manager's Perspective and the Engineer's Perspective; 4.2: Single Ports, Dual Ports, and ROM: The Compiler
4.3: Nonvolatile Memories: The Block 4.4: Special-Purpose Memories: The Custom; 4.5: Concepts for Further Study; 5: Other Functions; 5.1: Lesson from the Real World: The Manager's Perspective and the Engineer's Perspective; 5.2: Phase-Locked Loops, Power-On Resets, and Other Small-Scale Integration Analogs; 5.3: Low-Power Support Structures; 5.4: Stitching Structures; 5.4.1: Core-Fill Cells; 5.4.2: IO-Fill Cells; 5.4.3: DECAP Cells; 5.4.4: CMP-Fill Cells; 5.4.5: Spare Logic Cells; 5.4.6: Probe-Point Cells; 5.4.7: Antenna Diodes; 5.4.8: Test-Debug Diodes; 5.4.9: Others
5.5: Hard, Firm, and Soft Boxes 5.6: Concepts for Further Study; 6: Physical Views; 6.1: Lesson from the Real World: The Manager's Perspective and the Engineer's Perspective; 6.2: Picking an Architecture; 6.3: Measuring Density; 6.4: The Need and the Way to Work with Fabrication Houses; 6.5: Concepts for Further Study; 7: SPICE; 7.1: Lesson from the Real World: The Manager's Perspective and the Engineer's Perspective; 7.2: Why a Tool More Than 40 Years Old Is Still Useful; 7.3: Accuracy, Reality, and Why SPICE Results Must be Viewed with a Wary Eye; 7.4: Sufficient Parasitics
7.5: Concepts for Further Study 8: Timing Views; 8.1: Lesson from the Real World: The Manager's Perspective and the Engineer's Perspective; 8.2: Performance Limits and Measurement; 8.3: Default Versus Conditional Arcs; 8.4: Break-Point Optimization; 8.5: A Word on Setup and Hold; 8.6: Failure Mechanisms and Roll-Off; 8.7: Supporting Efficient Synthesis; 8.7.1: SPICE, Monotonic Arrays, and Favorite Stdcells; 8.7.2: SPICE, Positive Arrays, and Useful Skew; 8.8: Supporting Efficient Timing Closure; 8.9: Design Corner Specific Timing Views; 8.10: Nonlinear Timing Views are so ""Old Hat"" . . .
8.11: Concepts for Further Study

Sommario/riassunto

Shows readers how to gain the competitive edge in the integrated circuit marketplace This book offers a wholly unique perspective on the digital design kit. It points to hidden value in the safety margins of standard-cell libraries and shows design engineers and managers how to use this knowledge to beat the competition. Engineering the CMOS Library reveals step by step how the generic, foundry-provided standard-cell library is built, and how to extract value from existing std-cells and EDA tools in order to produce tighter-margined, smaller, faster, less power-hungry, and