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Nota di contenuto	Embedded SOPC Design with Nios II Processor and VHDL Examples; CONTENTS; Preface; Acknowledgments; 1 Overview of Embedded System; 1.1 Introduction; 1.1.1 Definition of an embedded system; 1.1.2 Example systems; 1.2 System design requirements; 1.3 Embedded SoPC systems; 1.3.1 Basic development flow; 1.4 Book organization; 1.5 Bibliographic notes; PART I BASIC DIGITAL CIRCUITS DEVELOPMENT; 2 Gate-level Combinational Circuit; 2.1 Overview of VHDL; 2.2 General description; 2.2.1 Basic lexical rules; 2.2.2 Library and package; 2.2.3 Entity declaration; 2.2.4 Data type and operators 2.2.5 Architecture body2.2.6 Code of a 2-bit comparator; 2.3 Structural description; 2.4 Testbench; 2.5 Bibliographic notes; 2.6 Suggested experiments; 2.6.1 Code for gate-level greater-than circuit; 2.6.2 Code for gate-level binary decoder; 3 Overview of FPGA and EDA Software; 3.1 FPGA; 3.1.1 Overview of a general FPGA device; 3.1.2 Overview of the Altera Cyclone II devices; 3.2 Overview of the Altera DE1 and DE2

boards; 3.3 Development flow; 3.4 Overview of Quartus II; 3.5 Short tutorial of Quartus II; 3.5.1 Create the design project; 3.5.2 Create a testbench and perform the RTL simulation
3.5.3 Compile the project3.5.4 Perform timing analysis; 3.5.5 Program the FPGA device; 3.6 Short tutorial on the ModelSim HDL simulator; 3.7 Bibliographic notes; 3.8 Suggested experiments; 3.8.1 Gate-level greater-than circuit; 3.8.2 Gate-level binary decoder; 4 RT-level Combinational Circuit; 4.1 RT-level components; 4.1.1 Relational operators; 4.1.2 Arithmetic operators; 4.1.3 Other synthesis-related VHDL constructs; 4.1.4 Summary; 4.2 Routing circuit with concurrent assignment statements; 4.2.1 Conditional signal assignment statement; 4.2.2 Selected signal assignment statement
4.3 Modeling with a process4.3.1 Process; 4.3.2 Sequential signal assignment statement; 4.4 Routing circuit with if and case statements; 4.4.1 If statement; 4.4.2 Case statement; 4.4.3 Comparison to concurrent statements; 4.4.4 Unintended memory; 4.5 Constants and generics; 4.5.1 Constants; 4.5.2 Generics; 4.6 Design examples; 4.6.1 Hexadecimal digit to seven-segment LED decoder; 4.6.2 Sign-magnitude adder; 4.6.3 Barrel shifter; 4.6.4 Simplified floating-point adder; 4.7 Bibliographic notes; 4.8 Suggested experiments; 4.8.1 Multi-function barrel shifter; 4.8.2 Dual-priority encoder
4.8.3 BCD incrementor4.8.4 Floating-point greater-than circuit; 4.8.5 Floating-point and signed integer conversion circuit; 4.8.6 Enhanced floating-point adder; 5 Regular Sequential Circuit; 5.1 Introduction; 5.1.1 D FF and register; 5.1.2 Synchronous system; 5.1.3 Code development; 5.2 HDL code of the basic storage elements; 5.2.1 D FF; 5.2.2 Register; 5.2.3 Register file; 5.2.4 SRAM; 5.3 Simple design examples; 5.3.1 Shift register; 5.3.2 Binary counter and variant; 5.4 Testbench for sequential circuits; 5.5 Timing analysis; 5.5.1 Timing parameters; 5.5.2 Timing considerations in Quartus II
5.6 Case study

Sommario/riassunto

The book is divided into four major parts. Part I covers HDL constructs and synthesis of basic digital circuits. Part II provides an overview of embedded software development with the emphasis on low-level I/O access and drivers. Part III demonstrates the design and development of hardware and software for several complex I/O peripherals, including PS2 keyboard and mouse, a graphic video controller, an audio codec, and an SD (secure digital) card. Part IV provides three case studies of the integration of hardware accelerators, including a custom GCD (greatest common divisor) circuit, a Mandelb