

1. Record Nr.	UNINA9910807489503321
Autore	Yang Mengfei
Titolo	Fault-tolerance techniques for spacecraft control computers // Mengfei Yang [et al.]
Pubbl/distr/stampa	Singapore : , : Wiley, , 2017
ISBN	1-119-10741-5 1-119-10739-3 1-119-10740-7
Descrizione fisica	1 online resource (373 pages) : color illustrations
Disciplina	629.47/42
Soggetti	Space vehicles - Control systems Fault-tolerant computing
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Translation of: Hang tian qi kong zhi ji suan ji rong cuop ji shu.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Title Page; Copyright Page; Contents; Brief Introduction; Preface; Chapter 1 Introduction; 1.1 Fundamental Concepts and Principles of Fault-tolerance Techniques ; 1.1.1 Fundamental Concepts; 1.1.2 Reliability Principles; 1.1.2.1 Reliability Metrics; 1.1.2.2 Reliability Model; 1.2 The Space Environment and Its Hazards for the Spacecraft Control Computer; 1.2.1 Introduction to Space Environment; 1.2.1.1 Solar Radiation; 1.2.1.2 Galactic Cosmic Rays (GCRs); 1.2.1.3 Van Allen Radiation Belt; 1.2.1.4 Secondary Radiation; 1.2.1.5 Space Surface Charging and Internal Charging. 1.2.1.6 Summary of Radiation Environment 1.2.1.7 Other Space Environments; 1.2.2 Analysis of Damage Caused by the Space Environment; 1.2.2.1 Total Ionization Dose (TID); 1.2.2.2 Single Event Effect (SEE); 1.2.2.3 Internal/surface Charging Damage Effect; 1.2.2.4 Displacement Damage Effect; 1.2.2.5 Other Damage Effect; 1.3 Development Status and Prospects of Fault Tolerance Techniques; References; Chapter 2 Fault-Tolerance Architectures and Key Techniques ; 2.1 Fault-tolerance Architecture ; 2.1.1 Module-level Redundancy Structures ; 2.1.2 Backup Fault-tolerance Structures. 2.1.2.1 Cold-backup Fault-tolerance Structures 2.1.2.2 Hot-backup Fault-tolerance Structures ; 2.1.3 Triple-modular Redundancy (TMR) Fault-tolerance Structures ; 2.1.4 Other Fault-tolerance Structures ; 2.2 Synchronization Techniques; 2.2.1 Clock

Synchronization System; 2.2.1.1 Basic Concepts and Fault Modes of the Clock Synchronization System; 2.2.1.2 Clock Synchronization Algorithm; 2.2.2 System Synchronization Method; 2.2.2.1 The Real-time Multi-computer System Synchronization Method ; 2.2.2.2 System Synchronization Method with Interruption. 2.3 Fault-tolerance Design with Hardware Redundancy 2.3.1 Universal Logic Model and Flow in Redundancy Design; 2.3.2 Scheme Argumentation of Redundancy; 2.3.2.1 Determination of Redundancy Scheme; 2.3.2.2 Rules Obeyed in the Scheme Argumentation of Redundancy; 2.3.3 Redundancy Design and Implementation; 2.3.3.1 Basic Requirements; 2.3.3.2 FDMU Design; 2.3.3.3 CSSU Design; 2.3.3.4 IPU Design; 2.3.3.5 Power Supply Isolation Protection; 2.3.3.6 Testability Design; 2.3.3.7 Others; 2.3.4 Validation of Redundancy by Analysis; 2.3.4.1 Hardware FMEA; 2.3.4.2 Redundancy Switching Analysis (RSA). 2.3.4.3 Analysis of the Common Cause of Failure; 2.3.4.4 Reliability Analysis and Checking of the Redundancy Power; 2.3.4.5 Analysis of the Sneak Circuit in the Redundancy Management Circuit; 2.3.5 Validation of Redundancy by Testing; 2.3.5.1 Testing by Failure Injection; 2.3.5.2 Specific Test for the Power of the Redundancy Circuit; 2.3.5.3 Other Things to Note; References; Chapter 3 Fault Detection Techniques; 3.1 Fault Model; 3.1.1 Fault Model Classified by Time; 3.1.2 Fault Model Classified by Space; 3.2 Fault Detection Techniques; 3.2.1 Introduction; 3.2.2 Fault Detection Methods for CPUs
