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Nota di contenuto	Front Cover; In Praise of Memory Systems: Cache, DRAM, Disk; Memory Systems Cache, DRAM, Disk; Copyright Page; Contents; Preface; Overview. On Memory Systems and Their Design; Ov.1 Memory Systems; Ov.2 Four Anecdotes on Modular Design; Ov.3 Cross-Cutting Issues; Ov.4 An Example Holistic Analysis; Ov.5 What to Expect; Part I. Cache; Chapter 1. An Overview of Cache Principles; 1.1 Caches, 'Caches,' and "Caches"; 1.2 Locality Principles; 1.3 What to Cache, Where to Put It, and How to Maintain It; 1.4 Insights and Optimizations; Chapter 2. Logical Organization 2.1 Logical Organization: A Taxonomy 2.2 Transparently Addressed Caches; 2.3 Non-Transparently Addressed Caches; 2.4 Virtual Addressing and Protection; 2.5 Distributed and Partitioned Caches; 2.6 Case Studies; Chapter 3. Management of Cache Contents; 3.1 Case Studies: On-Line Heuristics; 3.2 Case Studies: Off-Line Heuristics; 3.3 Case Studies: Combined Approaches; 3.4 Discussions; 3.5 Building a Content-Management; Chapter 4. Management of Cache Consistency;

4.1 Consistency with Backing Store; 4.2 Consistency with Self; 4.3 Consistency with Other Clients; Chapter 5. Implementation Issues 5.1 Overview 5.2 SRAM Implementation; 5.3 Advanced SRAM Topics; 5.4 Cache Implementation; Chapter 6. Cache Case Studies; 6.1 Logical Organization; 6.2 Pipeline Interface; 6.3 Case Studies of Detailed Itanium-2 Circuits; Part II. DRAM; Chapter 7. Overview of DRAMs; 7.1 DRAM Basics: Internals, Operation; 7.2 Evolution of the DRAM Architecture; 7.3 Modern-Day DRAM Standards; 7.4 Fully Buffered DIMM: A Compromise of Sorts; 7.5 Issues in DRAM Systems, Briefly; Chapter 8. DRAM Device Organization: Basic Circuits and Architecture; 8.1 DRAM Device Organization; 8.2 DRAM Storage Cells 8.3 RAM Array Structures 8.4 Differential Sense Amplifier; 8.5 Decoders and Redundancy; 8.6 DRAM Device Control Logic; 8.7 DRAM Device Configuration; 8.8 Data I/O; 8.9 DRAM Device Packaging; 8.10 DRAM Process Technology and Process Scaling Considerations; Chapter 9. DRAM System Signaling and Timing; 9.1 Signaling System; 9.2 Transmission Lines on PCBs; 9.3 Termination; 9.4 Signaling; 9.5 Timing Synchronization; 9.6 Selected DRAM Signaling and Timing Issues; 9.7 Summary; Chapter 10. DRAM Memory System Organization; 10.1 Conventional Memory System; 10.2 Basic Nomenclature; 10.3 Memory Modules 10.4 Memory System Topology 10.5 Summary; Chapter 11. Basic DRAM Memory-Access Protocol; 11.1 Basic DRAM Commands; 11.2 DRAM Command Interactions; 11.3 Additional Constraints; 11.4 Command Timing Summary; 11.5 Summary; Chapter 12. Evolutionary Developments of DRAM Device Architecture; 12.1 DRAM Device Families; 12.2 Historical-Commodity DRAM Devices; 12.3 Modern-Commodity DRAM Devices; 12.4 High Bandwidth Path; 12.5 Low Latency; 12.6 Interesting Alternatives; Chapter 13. DRAM Memory Controller; 13.1 DRAM Controller Architecture; 13.2 Row-Buffer-Management Policy 13.3 Address Mapping (Translation)

Sommario/riassunto

Bones and Cartilage provides the most in-depth review ever assembled on the topic. It examines the function, development and evolution of bone and cartilage as tissues, organs and skeletal systems. It describes how bone and cartilage is developed in embryos and are maintained in adults, how bone reappears when we break a leg, or even regenerates when a newt grows a new limb, or a lizard a tail. This book also looks at the molecules and cells that make bones and cartilages and how they differ in various parts of the body and across species. It answers such questions as "Is bone always
