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Nota di contenuto	NANO-CMOS CIRCUIT AND PHYSICAL DESIGN; CONTENTS; FOREWORD; PREFACE; 1 NANO-CMOS SCALING PROBLEMS AND IMPLICATIONS; 1.1 Design Methodology in the Nano-CMOS Era; 1.2 Innovations Needed to Continue Performance Scaling; 1.3 Overview of Sub-100-nm Scaling Challenges and Subwavelength Optical Lithography; 1.3.1 Back-End-of-Line Challenges (Metallization); 1.3.2 Front-End-of-Line Challenges (Transistors); 1.4 Process Control and Reliability; 1.5 Lithographic Issues and Mask Data Explosion; 1.6 New Breed of Circuit and Physical Design Engineers; 1.7 Modeling Challenges 1.8 Need for Design Methodology Changes1.9 Summary; References; PART I PROCESS TECHNOLOGY AND SUBWAVELENGTH OPTICAL LITHOGRAPHY: PHYSICS, THEORY OF OPERATION, ISSUES, AND SOLUTIONS; 2 CMOS DEVICE AND PROCESS TECHNOLOGY; 2.1 Equipment Requirements for Front-End Processing; 2.1.1 Technical Background; 2.1.2 Gate Dielectric Scaling; 2.1.3 Strain Engineering; 2.1.4 Rapid Thermal Processing Technology; 2.2 Front-End-Device Problems in CMOS Scaling; 2.2.1 CMOS Scaling Challenges; 2.2.2 Quantum Effects Model; 2.2.3 Polysilicon Gate Depletion Effects; 2.2.4

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Sommario/riassunto

Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and low power with leaky transistors; and DFM, yield, and the impact of physical implementation.