1. Record Nr. UNINA9910796564203321

Autore	Murad Khurram
Titolo	Inter personal relations : an Islamic perspective / / Khurram Murad ; edited by Abdur Rashid Siddiqui
Pubbl/distr/stampa	Leicestershire : , : The Islamic Foundation, , [2005] ©2005
Descrizione fisica	1 online resource (47 pages)
Disciplina	297.3
Soggetti	Interpersonal relations - Religious aspects - Islam
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9910438056903321

Autore	Gangadharan Sridhar
Titolo	Constraining designs for synthesis and timing analysis : a practical guide to synopsys design constraints (SDC) / / Sridhar Gangadharan, Sanjay Churiwala
Pubbl/distr/stampa	New York, : Springer, c2013
ISBN	1-4614-3269-3
Edizione	[1st ed. 2013.]
Descrizione fisica	1 online resource (245 p.)
Altri autori (Persone)	ChuriwalaSanjay
Disciplina	004.1 620 621.381 621.3815
Soggetti	Timing circuits Time measurements
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.

Nota di contenuto	Introduction -- Synthesis Basics -- Timing Analysis and Constraints -- SDC Extensions through Tcl -- Clocks -- Generated Clocks -- Clock Groups -- Other Clock Characteristics -- Port Delays -- Completing Port Constraints -- False Paths -- Multi Cycle Paths -- Combinatorial Paths -- Modal Analysis -- Managing Your Constraints -- Miscellaneous SDC Commands -- XDC: Xilinx Extensions To SDC.
Sommario/riassunto	This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints. · Provides a hands-on guide to synthesis and timing analysis, using Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints; · Includes key topics of interest to a synthesis, static timing analysis or place and route engineer; · Explains which constraints command to use for ease of maintenance and reuse, given several options possible to achieve the same effect on timing; · Explains fundamental concepts and provides exact command syntax.