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Sommario/riassunto	Long description: The continuous improvement in semiconductor technology requires field effect transistor scaling while maintaining acceptable leakage currents. This study analyzes the effect of scaling on the leakage current and defect distribution in peripheral DRAM transistors. The influence of important process changes, such as the high-k gate patterning and encapsulation as well as carbon co-implants in the source/drain junction are investigated by advanced electrical measurements and TCAD simulation. A complete model for the trap assisted leakage currents in the silicon bulk of the transistors is presented.