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	Nota di contenuto	Front Cover; The Definitive Guide to the ARM Cortex-M0; Copyright; Contents; Foreword; Preface; Acknowledgments; Conventions; Terms and Abbreviations; Chapter 1 Introduction; Why Cortex-M0?; Application of the Cortex-M0 Processors; Background of ARM and ARM processors; Cortex-M0 Processor Specification and ARM Architecture; ARM Processors and the ARM Ecosystem; Getting Started with the Cortex-M0 Processor; Organization of This Book and Resources; Chapter 2 Cortex-M0 Technical Overview; General Information on the Cortex-M0 Processor; The ARM Cortex-M0 Processor Features Advantages of the Cortex-M0 ProcessorLow-Power Applications; Cortex-M0 Software Portability; Chapter 3 Architecture; Overview; Programmer's Model; Memory System Overview; Stack Memory Operations; Exceptions and Interrupts; Nested Vectored Interrupt Controller (NVIC); System Control Block (SCB); Program Image and Startup Sequence; Chapter 4 Introduction to Cortex-M0 Programming; Introduction to Embedded System Programming; Inputs and Outputs; Development Flow; C Programming and Assembly Programming; What Is in a Program Image?; C Programming: Data Types; Accessing Peripherals in C

Cortex Microcontroller Software Interface Standard (CMSIS)Benefits of CMSIS; Chapter 5 Instruction Set; Background of ARM and Thumb Instruction Set; Assembly Basics; Pseudo Instructions; Chapter 6 Instruction Usage Examples; Overview; Program Control; Data Accesses; Data Type Conversion; Data Processing; Chapter 7 Memory System; Overview; Memory Map; Program Memory, Boot Loader, and Memory Remapping; Data Memory; Little Endian and Big Endian Support; Memory Attributes; Chapter 8 Exceptions and Interrupts; What Are Exceptions and Interrupts?; Exception Types on the Cortex-M0 Processor

Exception Priority DefinitionVector Table; Exception Sequence Overview; EXC_RETURN; Details of Exception Entry Sequence; Details of Exception Exit Sequence; Chapter 9 Interrupt Control and System Control; Overview of the NVIC and System Control Block Features; Interrupt Enable and Clear Enable; Interrupt Pending and Clear Pending; Interrupt Priority Level; Generic Assembly Code for Interrupt Control; Exception Masking Register (PRIMASK); Interrupt Inputs and Pending Behavior; Interrupt Latency; Control Registers for System Exceptions; System Control Registers

Chapter 10 Operating System Support FeaturesOverview of the OS Support Features; The SysTick Timer; SysTick Registers; Process Stack and Process Stack Pointer; SVC; PendSV; Chapter 11 Low-Power Features; Low-Power Embedded System Overview; Low-Power Advantages of the Cortex-M0 Processor; Overview of the Low-Power Features; Sleep Modes; Wait-for-Event (WFE) and Wait-for-Interrupt (WFI); Sleep-on-Exit Feature; Wakeup Interrupt Controller; Chapter 12 Fault Handling; Fault Exception Overview; Analyze a Fault; Accidental Switching to ARM State; Error Handling in Real Applications; Lockup Preventing Lockup

Sommario/riassunto	* Provides engineers with a thorough understanding of how the architecture works by giving detailed information on the processor architecture, including programmer's model instruction set and interrupt handling * Many examples of programming the Cortex-M0, in both C language and assembly language, gives engineers the 'up-and-running' they are looking for, quickly * Information on the software development flow including examples from various development tools for optimum efficiency * Information regarding software porting from other processor architectures including othe