| 1. | Record Nr. | UNISA996387546803316 |
|---|---|---|
| | Autore | Binning Hugh <1627-1653.> |
| | Titolo | The common principles of Christian religion, clearly proved, and singularly improved: or, a practical catechism [[electronic resource] ] : Wherein some of the most concerning foundations of our faith are solidly laid down; and that doctrine, which is according to godliness, sweetly, yet pungently pressed home, and most satisfyingly handled. / / By that worthy and faithful servant of Jesus Christ, Mr Hugh Binning, late minister of the gospel at Goven |
| | Pubbl/distr/stampa | Edinburgh, : Printed by George Swintoun, James Glen, and Thomas Brown, 1671 |
| | Edizione | [The 6. impression corrected and amended.] |
| | Descrizione fisica | [24], 252 p |
| | Soggetti | Christian life - 17th century <br> Christian life <br> Christian life - Presbyterian authors |
| | Lingua di pubblicazione | Inglese |
| | Formato | Materiale a stampa |
| | Livello bibliografico | Monografia |
| | Note generali | Leaf preceding title page has on recto letter A surrounded by decorative border, and on verso an imprimatur. <br> 25 sermons by Hugh Binning. <br> Text continuous despite pagination. <br> Imperfect: tightly bound with some loss of text. <br> Page 236 misnumbered "238"; p.240 misnumbered "250" and p.244-245 misnumbered "246-247".  Page numbers repeated in their correct place. <br> Reproduction of the original in the National Library of Scotland. |
| | Sommario/riassunto | eebo-0097 |

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|---|---|---|
| 2. | Record Nr. | UNINA9910787492903321 |
| | Autore | Goel Ashok K. <1953-> |
| | Titolo | A one-semester course in modeling of VLSI interconnections / / Ashok K. Goel |
| | Pubbl/distr/stampa | New York, NY : , : Momentum Press, , [2015]<br>©2015 |
| | ISBN | 1-60650-513-0 |
| | Descrizione fisica | 1 online resource (362 p.) |
| | Collana | Electronic circuits and semiconductor devices collection |
| | Disciplina | 621.395 |
| | Soggetti | Integrated circuits - Very large scale integration - Mathematical models |
| | Lingua di pubblicazione | Inglese |
| | Formato | Materiale a stampa |
| | Livello bibliografico | Monografia |
| | Note generali | Description based upon print version of record. |
| | Nota di bibliografia | Includes bibliographical references and index. |
| | Nota di contenuto | 1. Introductory concepts -- 1.1 Metallic interconnections -- 1.2 Simplified modeling of resistive interconnections as ladder networks -- 1.3 Propagation modes in a metallic interconnection -- 1.4 Slow-wave mode -- 1.5 Propagation delays --<br>2. Modeling of interconnection resistances, capacitances, and inductances -- 2.1 Interconnection resistance -- 2.2 Modeling of resistance for a copper interconnection -- 2.3 Interconnection capacitances -- 2.4 The Green's function method, Method of images -- 2.5 Green's function method, Fourier integral approach -- 2.6 Interconnection inductances -- 2.7 Inductance extraction using FastHenry -- 2.8 Approximate equations for capacitances -- 2.9 Approximate equations for interconnection capacitances and inductances on silicon and GaAs substrates --<br>3. Modeling of interconnection delays -- 3.1 Metal-insulator-semiconductor microstrip line model of an interconnection -- 3.2 Transmission line analysis of single-level interconnections -- 3.3 Transmission line model for multilevel interconnections -- 3.4 Modeling of parallel and crossing interconnections -- 3.5 Modeling of very-high-frequency losses in interconnections -- 3.6 Compact modeling of interconnection delays -- 3.7 Modeling of active interconnections --<br>4. Modeling of interconnection crosstalk -- 4.1 Lumped capacitance model -- 4.2 Coupled multiconductor MIS microstrip line model -- 4.3 |

| Sommario/riassunto | Quantitative understanding of the parasitic capacitances and inductances and the resultant propagation delays and crosstalk phenomena associated with the metallic interconnections on the very large scale integrated (VLSI) circuits has become extremely important for the optimum design of the state-of-the-art integrated circuits. It is because more than 65 percent of the delays on the integrated circuit chip occur in the interconnections and not in the transistors on the chip. Mathematical techniques to model the parasitic capacitances, inductances, propagation delays, crosstalk noise, and electromigration-induced failure associated with the interconnections in the realistic high-density environment on a chip will be discussed. An overview of the future interconnection technologies for the nanotechnology circuits will also be presented. This book will be the first book of its kind written for a one-semester course on the mathematical modeling of metallic interconnections on a VLSI circuit. In most institutions around the world offering BS, MS, and Ph.D. degrees in Electrical and Computer Engineering, such a course will be suitable for the first-year graduate students and it will also be appropriate as an elective course for senior level BS students. This book will also be of interest to practicing engineers in the field who are looking for a quick refresher on this subject. |