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Altri autori (Persone)	HauckScott DeHonAndre
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Nota di contenuto	Front Cover; Reconfigurable Computing; Copyright Page; Table of Contents; List of Contributors; Preface; Introduction; Part I: Reconfigurable Computing Hardware; Chapter 1. Device Architecture; 1.1 Logic-The Computational Fabric; 1.2 The Array and Interconnect; 1.3 Extending Logic; 1.4 Configuration; 1.5 Case Studies; 1.6 Summary; References; Chapter 2. Reconfigurable Computing Architectures; 2.1 Reconfigurable Processing Fabric Architectures; 2.2 RPF Integration into Traditional Computing Systems; 2.3 Summary and Future Work; References; Chapter 3. Reconfigurable Computing Systems 3.1 Early Systems3.2 PAM, VCC, and Splash; 3.3 Small-Scale Reconfigurable Systems; 3.4 Circuit Emulation; 3.5 Accelerating Technology; 3.6 Reconfigurable Supercomputing; 3.7 Non-FPGA Research; 3.8 Other System Issues; 3.9 The Future of Reconfigurable Systems; References; Chapter 4. Reconfiguration Management; 4.1 Reconfiguration; 4.2 Configuration Architectures; 4.3 Managing the Reconfiguration Process; 4.4 Reducing Configuration Transfer Time; 4.5 Configuration Security; 4.6 Summary; References; Part II: Programming Reconfigurable Systems; Chapter 5. Compute Models and

System Architectures

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8.3 Specifying Control in Simulink 8.4 Component Reuse: Libraries of Simple and Complex Subsystems; 8.5 Summary; References; Chapter 9. Stream Computations Organized for Reconfigurable Execution; 9.1 Programming; 9.2 System Architecture and Execution Patterns; 9.3 Compilation; 9.4 Runtime; 9.5 Highlights; References; Chapter 10. Programming Data Parallel FPGA Applications Using the SIMD/Vector Model; 10.1 SIMD Computing on FPGAs: An Example; 10.2 SIMD Processing Architectures; 10.3 Data Parallel Languages; 10.4 Reconfigurable Computers for SIMD/Vector Processing
10.5 Variations of SIMD/Vector Computing 10.6 Pipelined SIMD/Vector Processing; 10.7 Summary; References; Chapter 11. Operating System Support for Reconfigurable Computing; 11.1 History; 11.2 Abstracted Hardware Resources; 11.3 Flexible Binding; 11.4 Scheduling; 11.5 Communication; 11.6 Synchronization; 11.7 Protection; 11.8 Summary; References; Chapter 12. The JHDL Design and Debug System; 12.1 JHDL Background and Motivation; 12.2 The JHDL Design Language; 12.3 The JHDL CAD System; 12.4 JHDL'S Hardware Mode; 12.5 Advanced JHDL Capabilities; 12.6 Summary; References
Part III: Mapping Designs to Reconfigurable Platforms

Sommario/riassunto

Reconfigurable Computing marks a revolutionary and hot topic that bridges the gap between the separate worlds of hardware and software design- the key feature of reconfigurable computing is its groundbreaking ability to perform computations in hardware to increase performance while retaining the flexibility of a software solution. Reconfigurable computers serve as affordable, fast, and accurate tools for developing designs ranging from single chip architectures to multi-chip and embedded systems. Scott Hauck and Andre DeHon have assembled a group of the key experts in the fields
