1. Record Nr. UNINA9910784132003321

Autore	Walen Denise A
Titolo	Constructions of female homoeroticism in early modern drama [[electronic resource] /] / Denise A. Walen
Pubbl/distr/stampa	New York, : Palgrave Macmillan, 2005
ISBN	1-281-36467-3 9786611364670 1-4039-8106-X
Edizione	[1st ed.]
Descrizione fisica	1 online resource (241 p.)
Collana	Early modern cultural studies
Disciplina	822/.309353
Soggetti	English drama - Early modern and Elizabethan, 1500-1600 - History and criticism Homosexuality and literature - England - History - 16th century Homosexuality and literature - England - History - 17th century English drama - 17th century - History and criticism Lesbians in literature Women in literature
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references (p. [201]-219) and index.
Nota di contenuto	Cover; Contents; Acknowledgments; Introduction; 1 The Eidolic Lesbian in Early Modern England; 2 Playfully Emergent Lesbian Erotics; 3 Anxiously Emergent Lesbian Erotics; 4 Predatory Lesbian Erotics; 5 Utopian Lesbian Erotics; Conclusion; Appendix: List of Plays; Notes; Bibliography; Index
Sommario/riassunto	This book explores representations of love and desire between female characters in nearly seventy plays written between 1580 and 1660. The work argues that playwrights of late sixteenth- and early seventeenth-century England recognized and constructed richly diverse tropes of female homoerotic desire. Writers place female characters in erotic situations with other female characters in playful scenarios of mistaken identity, in anxious moments of amorous intrigue, in predatory situations and in enthusiastic, utopian representations of romantic love. These plays indicate an awareness of female homoeroticism in early modern England and belie statements that literary evidence of

homosexuality was concerned primarily with men.

2. Record Nr. UNINA9910784654303321

Autore	Leibson Steve
Titolo	Designing SOCs with configured cores [[electronic resource]] : unleashing the Tensilica Xtensa and diamond cores / / Steve Leibson
Pubbl/distr/stampa	Amsterdam ; ; Boston, : Morgan Kaufmann Publishers, c2006
ISBN	1-280-96685-8 9786610966851 0-08-047245-1
Edizione	[1st edition]
Descrizione fisica	1 online resource (341 p.)
Collana	The Morgan Kaufmann series in systems on silicon
Disciplina	621.3815
Soggetti	Embedded computer systems - Design and construction Systems on a chip - Design and construction
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Front Cover; About the Author; Title page; Copyright Page; Table of contents; Foreword; Preface; Acknowledgements; 1 Introduction to 21st-Century SOC Design; 1.1 The Start of Something Big; 1.2 Few Pins = Massive Multiplexing; 1.3 Third Time's a Charm; 1.4 The Microprocessor: A Universal System Building Block; 1.5 The Consequences of Performance-in the Macro World; 1.6 Increasing Processor Performance in the Micro World; 1.7 I/O Bandwidth and Processor Core Clock Rate; 1.8 Multitasking and Processor Core Clock Rate; 1.9 System-Design Evolution 1.10 Heterogeneous- and Homogeneous-Processor System-Design Approaches1.11 The Rise of MPSOC Design; 1.12 Veering Away from Processor Multitasking in SOC Design; 1.13 Processors: The Original, Reusable Design Block; 1.14 A Closer Look at 21st-Century Processor Cores for SOC Design; Bibliography; 2 The SOC Design Flow; 2.1 System-Design Goals; 2.2 The ASIC Design Flow; 2.3 The ad-hoc SOC Design Flow; 2.4 A Systematic MPSOC Design Flow; 2.5 Computational Alternatives; 2.6 Communication Alternatives; 2.7 Cycle-Accurate

System Simulation; 2.8 Detailed Implementation
2.9 Summary: Handling SOC ComplexityBibliography; 3 Xtensa Architectural Basics; 3.1 Introduction to Configurable Processor Architectures; 3.2 Xtensa Registers; 3.3 Register Windowing; 3.4 The Xtensa Program Counter; 3.5 Memory Address Space; 3.6 Bit and Byte Ordering; 3.7 Base Xtensa Instructions; 3.8 Benchmarking the Xtensa Core ISA; Bibliography; 4 Basic Processor Configurability; 4.1 Processor Generation; 4.2 Xtensa Processor Block Diagram; 4.3 Pre-Configured Processor Cores; 4.4 Basics of TIE; 4.5 TIE Instructions; 4.6 Improving Application Performance Using TIE
4.7 TIE Registers and Register Files4.8 TIE Ports; 4.9 TIE Queue Interfaces; 4.10 Combining Instruction Extensions with Queues; 4.11 Diamond Standard Series Processor Cores-Dealing with Complexity; Bibliography; 5 MPSOC System Architectures and Design Tools; 5.1 SOC Architectural Evolution; 5.2 The Consequences of Architectural Evolution; 5.3 Memory Interfaces; 5.4 Memory Caches; 5.5 Local ROM and Local RAM Interfaces, the XLMI Port, and the PIF; 5.6 The PIF; 5.7 Ports and Queue Interfaces; 5.8 SOC Connection Topologies; 5.9 Shared-Memory Topologies; 5.10 Direct Port-Connected Topologies
5.11 Queue-Based System Topologies5.12 Existing Design Tools for Complex SOC Designs; 5.13 MPSOC Architectural-Design Tools; 5.14 Platform Design; 5.15 An MPSOC-Design Tool; 5.16 MPSOC System-Level Simulation Example; 5.17 SOC Design in the 21st Century; Bibliography; 6 Introduction to Diamond Standard Series Processor Cores; 6.1 The Diamond Standard Series of 32-bit Processor Cores; 6.2 Diamond Standard Series Software-Development Tools; 6.3 Diamond Standard Series Feature Summary; 6.4 Diamond Standard Series Processor Core Hardware Overview and Comparison
6.5 Diamond-Core Local-Memory Interfaces

Sommario/riassunto

Microprocessor cores used for SOC design are the direct descendents of Intel's original 4004 microprocessor. Just as packaged microprocessor ICs vary widely in their attributes, so do microprocessors packaged as IP cores. However, SOC designers still compare and select processor cores the way they previously compared and selected packaged microprocessor ICs. The big problem with this selection method is that it assumes that the laws of the microprocessor universe have remained unchanged for decades. This assumption is no longer valid.Processor cores for SOC designs can be far more plas