1. Record Nr. UNINA990001026070403321

Autore	Lighstone, A.H.
Titolo	Symbolic Logic and the Real Number Systems : An Introduction to the Foundations of Number Systems / A.H. Lightstone
Pubbl/distr/stampa	New York : Harper & Row, 1966
Disciplina	512 513
Locazione	FI1
Collocazione	9-001
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9910679888503321

Autore	Bond Robert (Robert T. J.)
Titolo	Negotiating tactics and techniques for software & Hi-Tech agreements / / Robert Bond
Pubbl/distr/stampa	London : , : Hawksmere, , [1998] ©1998
ISBN	1-85418-563-2
Descrizione fisica	1 online resource (229 p.)
Disciplina	343.410999
Soggetti	Negotiation in business Acquisition of computer software - Management Requests for proposals (Public contracts)
Lingua di pubblicazione	Inglese
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Note generali	Description based upon print version of record.
Nota di contenuto	Acknowledgements; Author; Preface; Contents; 1. Understanding negotiating principles; 2. Preparing for negotiation; 3. Memoranda of Understanding and Heads Agreement; 4. Getting the content right; 5.

Overcoming classic obstacles and obstructions; 6. Tactics of customers; 7. Further customers negotiating tactics; 8. Creative problem solving; 9. The use of non-verbals in negotiation; appendices; Appendix A Case study; Appendix B Heads of Agreement for software distribution; Appendix C Multimedia product licence and distribution agreement; Appendix D Software Escrow agreement (multiple licensee) Appendix E Patent licenceAppendix F Non-disclosure undertaking; Appendix G Confidentiality letter; Appendix H Confidentiality and non-disclosure agreement; Appendix I Disputes and law; Appendix J Sample Invitation to Tender (ITT); Glossary; Recommended reading

Sommario/riassunto

What does negotiating in the hi-tech sector involve? The hi-tech sector is different. Commercial negotiations tend to cover all aspects of the transaction, not just issues such as price, performance and deadlines. The high value attributable to the intellectual property element of technology transfer transactions adds an additional dimension. The sheer internationalism of sectors such as information technology, telecommunications, biotech and pharmaceutical technology increase the complexity of the cultural and legal issues that are relevant to the negotiator. How will this Report help your bu

3. Record Nr. UNINA9910784350603321

Autore	Yiu Joseph
Titolo	The definitive guide to the ARM Cortex-M3 [[electronic resource] /] / Joseph Yiu
Pubbl/distr/stampa	Amsterdam ; ; Boston, : Newnes, c2007
ISBN	1-281-03935-7 9786611039356 0-08-055143-2
Edizione	[1st edition]
Descrizione fisica	1 online resource (380 p.)
Collana	Embedded technology series
Disciplina	004.16 004.256
Soggetti	Embedded computer systems Microprocessors
Lingua di pubblicazione	Inglese
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Livello bibliografico	Monografia
Note generali	Includes bibliographical references (p. xix) and index.
Nota di contenuto	Front Cover; The Definitive Guide to the ARM Cortex-M3; Copyright Page; Table of Contents; Foreword; Preface; Acknowledgments; Terms and Abbreviations; Conventions; References; Chapter 1 - Introduction; What Is the ARM Cortex-M3 Processor?; Background of ARM and ARM Architecture; A Brief History; Architecture Versions; Processor Naming; Instruction Set Development; The Thumb-2 Instruction Set Architecture (ISA); Cortex-M3 Processor Applications; Organization of This Book; Further Readings; Chapter 2 - Overview of the Cortex-M3; Fundamentals; Registers; R0 to R12: General-Purpose Registers R13: Stack PointersR14: The Link Register; R15: The Program Counter; Special Registers; Operation Modes; The Built-In Nested Vectored Interrupt Controller; Nested Interrupt Support; Vectored Interrupt Support; Dynamic Priority Changes Support; Reduction of Interrupt Latency; Interrupt Masking; The Memory Map; The Bus Interface; The Memory Protection Unit; The Instruction Set; Interrupts and Exceptions; Debugging Support; Characteristics Summary; High Performance; Advanced Interrupt-Handling Features; Low Power Consumption; System Features; Debug Supports; Chapter 3 - Cortex-M3 Basics RegistersGeneral-Purpose Registers R0-R7; General-Purpose Registers

R8-R12; Stack Pointer R13; Link Register R14; Program Counter R15; Special Registers; Program Status Registers (PSRs); PRIMASK, FAULTMASK, and BASEPRI Registers; The Control Register; Operation Mode; Exceptions and Interrupts; Vector Tables; Stack Memory Operations; Basic Operations of the Stack; Cortex-M3 Stack Implementation; The Two-Stack Model in the Cortex-M3; Reset Sequence; Chapter 4 - Instruction Sets; Assembly Basics; Assembler Language: Basic Syntax; Assembler Language: Use of Suffixes Assembler Language: Unified Assembler LanguageInstruction List; Unsupported Instructions; Instruction Descriptions; Assembler Language: Moving Data; LDR and ADR Pseudo Instructions; Assembler Language: Processing Data; Assembler Language: Call and Unconditional Branch; Assembler Language: Decisions and Conditional Branches; Assembler Language: Combined Compare and Conditional Branch; Assembler Language: Conditional Branches Using IT Instructions; Assembler Language: Instruction Barrier and Memory Barrier Instructions; Assembly Language: Saturation Operations Several Useful Instructions in the Cortex-M3MSR and MRS; IF-THEN; CBZ and CBNZ; SDIV and UDIV; REV, REVH, and REVSH; RBIT; SXTB, SXTH, UXTB, and UXTH; BFC and BFI; UBFX and SBFX; LDRD and STRD; TBB and TBH; Chapter 5 - Memory Systems; Memory System Features Overview; Memory Maps; Memory Access Attributes; Default Memory Access Permissions; Bit-Band Operations; Advantages of Bit-Band Operations; Bit-Band Operation of Different Data Sizes; Bit-Band Operations in C Programs; Unaligned Transfers; Exclusive Accesses; Endian Mode; Chapter 6 - Cortex-M3 Implementation Overview; The Pipeline
A Detailed Block Diagram

Sommario/riassunto

This user's guide does far more than simply outline the ARM Cortex-M3 CPU features; it explains step-by-step how to program and implement the processor in real-world designs. It teaches readers how to utilize the complete and thumb instruction sets in order to obtain the best functionality, efficiency, and reuseability. The author, an ARM engineer who helped develop the core, provides many examples and diagrams that aid understanding. Quick reference appendices make locating specific details a snap! Whole chapters are dedicated to: Debugging using the new CoreSight technologyMi